Siemens Nixdorf

MCM-21P2

GENERIC SAFETY PRECAUTIONS

WARNING: The following precautions must be observed

ALL PRODUCTS

Before any service is performed on the chassis an isolation transformer should be inserted between the power line and the product.

1. When replacing the chassis in the cabinet, ensure all the protective devices are put back in place.
2. When service is required, observe the original lead dressing. Extra precaution should be taken to ensure correct lead dressing in any high voltage circuitry area.
3. Many electrical and mechanical parts in HITACHI products have special safety related characteristics. These characteristics are often not evident from visual inspection, nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified by marking with a ⚠ on the schematics and the replacement parts list. The use of a substitute replacement component that does not have the same safety characteristics as the HITACHI recommended replacement one, shown in the parts list, may create electrical shock, fire, X-radiation, or other hazards.
4. Always replace original spacers and maintain lead lengths. Furthermore, where a short circuit has occurred, replace those components that indicate evidence of overheating.
5. Insulation resistance should not be less than 2M ohms at 500V DC between the main poles and any accessible metal parts.
6. No flashover or breakdown should occur during the dielectric strength test, applying 3kV AC or 4.25kV DC for two seconds between the main poles and accessible metal parts.
7. Before returning a serviced product to the customer, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. The service technician must make sure that no protective device built into the instrument by the manufacturer has become defective, or inadvertently damaged during servicing.

CE MARK

1. HITACHI products may contain the CE mark on the rating plate indicating that the product contains parts that have been specifically approved to provide electromagnetic compatibility to designated levels.
2. When replacing any part in this product, please use only the correct part itemised in the parts list to ensure this standard is maintained, and take care to replace lead dressing to its original state, as this can have a bearing on the electromagnetic radiation/immunity.

PICTURE TUBE

1. The line output stage can develop voltages in excess of 25kV; if the E.H.T. cap is required to be removed, discharge the anode to chassis via a high value resistor, prior to its removal from the picture tube.
2. High voltage should always be kept at the rated value of the chassis and no higher. Operating at higher voltages may cause a failure of the picture tube or high voltage supply, and also, under certain circumstances could produce X-radiation levels moderately in excess of design levels. The high voltage must not, under any circumstances, exceed 29kV on the chassis (except for projection Televisions).
3. The primary source of X-radiation in the product is the picture tube. The picture tube utilised for the above mentioned function in this chassis is specially constructed to limit X-radiation. For continued X-radiation protection, replace tube with the same type as the original HITACHI approved type
4. Keep the picture tube away from the body while handling. Do not install, remove, or handle the picture tube in any manner unless shatterproof goggles are worn. People not so equipped should be kept away while picture tubes are handled

LASERS

If the product contains a laser avoid direct exposure to the beam when the cover is open or when interlocks are defeated or have failed.

FEATURES

1. Flat screen CRT with anti-glare, dynamic focus circuit,dark glass, and INVAR shadow mask give the sharpest focus and highest contrast.
2. Automatic scanning and automatic adjustment to conform with a wide range of scanning frequencies and user requirements.
3. Signal input allows D-Sub Min 15pin cable.
4. Power Save Mode automatically puts the monitor into a standby mode (power consumption less than 15W) when the H.sync. signal is not detected, and a power - off mode(less than 5W) when the V.sync, signal is not detected. Normal mode is restored immediately when the H. sync. signal and the V.sync signal are detected. This feature prolongs monitor life and reduces energy consumption by up to about 75%.

SAFETY PRECAUTIONS

NOTICE: Comply with all cautions and safety related notes located on or inside the cabinet and on the chassis or picture tube.

The following precautions must be observed.

1. Do not install, remove, or handle the picture tube in any manner unless shatterproof goggles are worn. People not so equipped should be kept away while picture tubes are handled.
2. When replacing a chassis in the monitor, all the protective devices must be put back in place, such as, barriers, non-metallic knobs, adjustment and compartment shields, and isolation resistor-capacitor, etc.
3. When service is required, observe the original lead dress. Extra precaution should be taken to assure correct lead dress in the high voltage circuitry area.
4 Always use the manufacturer's replacement components. Especially critical components as indicated on the circuit diagram should not be replaced by other manufacturer's. Furthermore where a short circuit has occurred, replace those components that indicate evidence of overheating.
5. Before returning a serviced monitor to the customer, the service personnel must thoroughly test unit to be certain that it is completely safe to operate without danger of electrical shock, and be sure that no protective device built into the monitor by the manufacturer has become defective, or inadvertently defeated during servicing.
   Therefore, the following checks should be performed for continued protection of the customer and service technician.
6. In the case of the micro processor unit, shop adjustment is necessary after exchange of the micro processor unit.

High Voltage

This monitor is provided with a high voltage hold down circuit for clearly indicating that voltage has increased in excess of a predetermined value.

Comply with notes described in this Service Manual regarding this hold down circuit when servicing, so that this hold down circuit may function correctly.

Service Warning

With minimum Brightness and Contrast the operating high voltage in this display is lower than 30 kV.

If any component having influence on the high voltage is replaced, confirm that the high voltage with minimum Brightness and Contrast is lower than 30 kV.

To measure high voltage use a high impedance high voltage meter. (SENSITIVE RESEARCH Model: ESH or Equivalent)

Connect (-) to chassis earth and (+) to the CDT anode button. (See the following connection diagram Fig. 1.)

NOTE: Turn power switch off without fail before making the connection to the Anode button

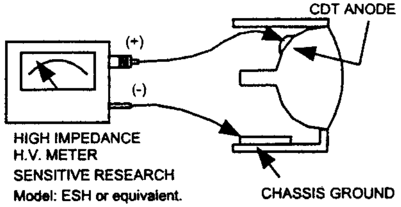


Fig. 1

X-radiation

TUBE: The source of X-radiation in this monitor is the picture tube. The tube utilized in this chassis is specially constructed to limit X-radiation emissions.

For continued X-radiation protection, the replacement tube must be the same type as the original, manufacturer approved type.

When troubleshooting and making test measurements in a monitor with a problem of excessive high voltage, avoid being unnecessarily close to the picture tube and the high voltage components.

Do not operate the chassis longer than is necessary to locate the cause of excessive voltage.

CHECK OF HIGH VOLTAGE HOLD DOWN CIRCUIT

Checking of the high Voltage hold down circuit operation.

1. Turn the switch of the unit ON, and set the Brightness and Contrast controls to max.
2. Turn the switch of the unit OFF.
3. Connect a DC Voltmeter and an adjustment jig as shown in Fig. 2.
4. Set the adjustment VR to fully counterclockwise.
5. Turn the switch of the unit ON and gradually rotate the adjustment VR clockwise.
6. Check that a reading of DC voltage-meter is less-than 0.6±0.1 V when picture disappears.
7. Turn the switch of the unit OFF immediately after checking that the picture disappears.
8. Remove the adjusting jig and the DC voltmeter.

NOTE: Reading of 0.6 V is approximately equivalent to 30 kV of CDT Anode High Voltage.

PRODUCT SAFETY NOTICE

Many electrical mechanical parts in the color monitor units have special safety related characteristics.
These are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.
Electrical components having such features are identified by marking with ⚠ on the schematics and on the parts list in this Service Manual.
The use of a substitute replacement component which does not have the same safety characteristics as the manufacturer recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, X-radiation, or other hazards.
Productions are issued from time to time. For the latest information, always consult this Service Manual.

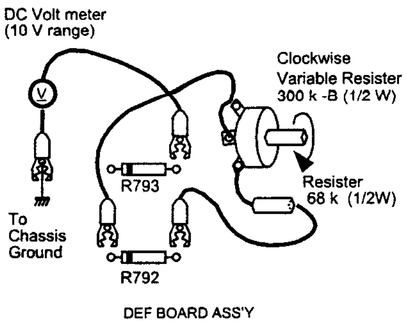
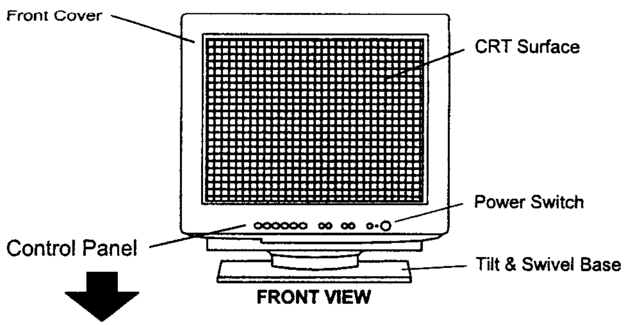

DC Volt meter
(10 V range)
V
Clockwise
Variable Resister
300 k -B (1/2 W)
R793
Resister
68 k (1/2W)
To
Chassis
Ground
R792
DEF BOARD ASS'Y

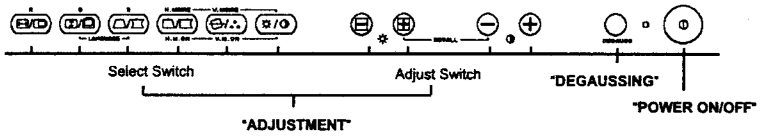
Fig. 2 Checking Circuit using jig

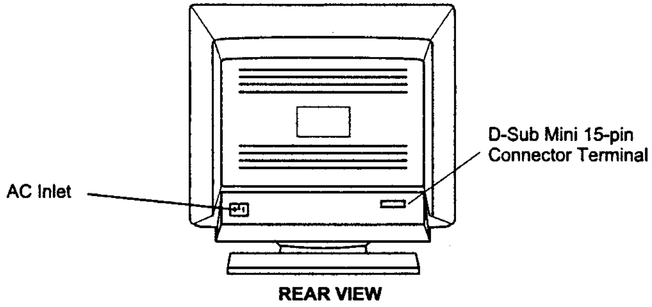
SPECIFICATIONS

Model Name		CM811*	CM812*		
Destination		North America (*="U") Europe (*="ET")	North America (*="U") Europe (*="ET")		
Rated Voltage		AC 100-120 / 200-240 V, Automatically select. Provided with Power Circuit.			
Power Consumption		125 W nominal			
Color Display Tube (CDT)		21inch inches diagonal, 0.22 mm horizontal dot pitch Invar shadow mask, Black matrix, Anti-Reflection coat, Short persistence phosphors.			
Rated Frequency	Horizontal	31 - 96 kHz	31 - 107 kHz		
	Vertical	50 - 160 Hz			
Resolution	Horizontal	Up to 1600			
	Vertical	Up to 1280			
Signal Inputs		Red, Green and Blue analog video H/V separate, H/V composite or Sync .on Green sync.			
User Controls		Power Switch Degauss Language selectContrast Brightness Horizontal Position, Size Vertical Position, Size Right Side Pincushion Right Trapezoid Side Pincushion Trapezoid Red,Green,Blue intensity Color Select Rotation H Moire Reduction V Moire Reduction			
Environmental Condition		Operation Temperature : 5 °C to 40 °C Humidity : 10% to 80%	Storage -20 to 60 °C 10% to 90 %		
Dimensions		488 (W) x 482 (H) x 470 (D) mm Including Tilt & Swivel base.			
Weight		27.5 kg			

CONTROLS


Front Cover
CRT Surface
Power Switch
Control Panel
Tilt & Swivel Base
FRONT VIEW


Select Switch
Adjust Switch
"DEGAUSSING"
"POWER ON/OFF"
"ADJUSTMENT"


D-Sub Mini 15-pin
Connector Terminal
AC Inlet
REAR VIEW

SIGNAL TIMING CHART

	Signal		VGA 640×400	VESA 800×600 (85Hz)	VESA 1024×768 (85Hz)	VGSA 1280×1024 (85Hz)
1	Video	Type	R/G/B Analog	R/G/B Analog	R/G/B Analog	R/G/B Analog
		Voltage	0.7 Vp-p	0.7 Vp-p	0.7 Vp-p	0.7 Vp-p
		Set Up	None	None	None	None
2	Sync	Type	H/V Separate	H/V Separate	H/V Separate	H/V Separate
		Amp.	TTL Level (Nega./Posi.)	TTL Level (Posi./Posi.)	TTL Level (Posi./Posi.)	TTL Level (Posi./Posi.)
3	Video frequency		25.175 MHz	56.250 MHz	94.500 MHz	157.500 MHz
4	Character (Letter)		640dots×400lines	800dots×600lines	1024dots×768lines	1280dots×1024lines
5	Horizontal	Frequency	31.469 kHz	53.674 kHz	68.677 kHz	91.146 kHz
		Front porch	0.636us (16cl)	0.569us (32cl)	0.508us (48cl)	0.406us (64cl)
		Sync. width	3.813us (96cl)	1.138us (64cl)	1.016us (96cl)	1.016us (160cl)
		Back porch	1.907us (48cl)	2.702us (152cl)	2.201us (208cl)	1.422us (224cl)
		Blanking widht	6.356us (160cl)	4.409us (248cl)	3.725us (352cl)	2.844us (448cl)
		Display time	25.422us (640cl)	14.222us (800cl)	10.836us (1024cl)	8.127us (280cl)
		H.period (1H)	31.778us (800cl)	18.631us (1048cl)	14.561us (1376cl)	10.971us (1728cl)
6	Vertical	Frequency	70.090 Hz	85.062 Hz	85.000Hz	85.024 Hz
		Front porch	0.381 ms (12H)	0.019 ms (1H)	0.015 ms (1H)	0.011ms (1H)
		Sync. width	0.064 ms (2H)	0.056 ms (3H)	0.044 ms (3H)	0.033 ms (3H)
		Back porch	1.112 ms (35H)	0.503 ms (27H)	0.524 ms (36H)	0.483 ms (44H)
		Blanking width	1.557 ms (49H)	0.578 ms (31H)	0.582 ms (40H)	0.527 ms (48H)
		Display time	12.711 ms (400H)	11.179 ms (600H)	11.183 ms (768H)	11.235 ms (1024H)
		H.period (1H)	14.268 ms (449H)	11.756 ms (631H)	11.765 ms (808H)	11.761 ms (1072H)
7	Scan System		(Non-interlaced)	(Non-interlaced)	(Non-interlaced)	(Non-interlaced)
8	Remark					
9	Signal name		30B	54A	68A	91A

- * VGA is a registered trademark of International Business Machined Corporation.
- * VESA is a trademark of a nonprofit organization, Video Electronics Standard Association.

	Signal		VESA 1600×1200 (75Hz)	VESA 1600×1200 (85Hz)	Macintosh II 1152×870 (75Hz)	fHLL Adjustment signal
1	Video	Type	R/G/B Analog	R/G/B Analog	R/G/B Analog	R/G/B Analog
		Voltage	0.7 Vp-p	0.7 Vp-p	0.7 Vp-p	0.7 Vp-p
		Set Up	None	None	None	None
2		Type	H/V Separate	H/V Separate	H/V Separate	H/V Separate
		Amp.	TTL Level (Posi./Posi.)	TTL Level (Posi./Posi.)	TTL Level (Nega./Nega.)	TTL Level (Nega./Nega.)
3	Video frequency		202.500 MHz	229.500 MHz	100.000 MHz	24.000 MHz
4	Character (Letter)		1600dots×1200lines	1600dots×1200lines	1152dots×870lines	640dots×410lines
5	Horizontal	Frequency	93.750 kHz	106.250 kHz	68.681 kHz	30.000 kHz
		Front porch	0.316us (64cl)	0.279us (64cl)	0.320us (32cl)	0.417us (10cl)
		Sync. width	0.948us (192cl)	0.837us (192cl)	1.280us (128cl)	3.917us (94cl)
		Back porch	1.501us (304cl)	1.325us (304cl)	1.440us (144cl)	2.333us (56cl)
		Blanking widht	2.765us (560cl)	2.440us (560cl)	3.040us (304cl)	6.667us (160cl)
		Display time	7.901us (1600cl)	6.972us (1600cl)	11.520us (1152cl)	26.667us (640cl)
		H.period (1H)	10.667us (2160cl)	9.412us (2160cl)	14.560us (1456cl)	33.333us (800cl)
6	Vertical	Frequency	75.000 Hz	85.000 Hz	75.060 Hz	50.000 Hz
		Front porch	0.011 ms (1H)	0.009 ms (1H)	0.044 ms (3H)	2.967 ms (89H)
		Sync. width	0.032ms (3H)	0.028ms (3H)	0.044ms (3H)	0.133ms (4H)
		Back porch	0.491 ms (46H)	0.433 ms (46H)	0.568 ms (39H)	3.233 ms (97H)
		Blanking widht	0.533 ms (50H)	0.471 ms (50H)	0.655 ms (45H)	6.333 ms (190H)
		Display time	12.800 ms (1200H)	11.294 ms (1200H)	12.667 ms (870H)	13.667 ms (410H)
		H.period (1H)	13.333 ms (1250H)	11.765 ms (1250H)	13.322 ms (915H)	20.000 ms (600H)
7	Scan System		(Non-interlaced)	(Non-interlaced)	(Non-interlaced)	(Non-interlaced)
8	Remark		only CM811*	only CM812*	only CM811ET	
9	Signal name		94A	106B	70A	30W

- * Macintosh II is a trademark of Apple Computer,Inc

DISCRIPTION OF CIRCUIT

1. Power Supply Circuit

This model incorporates a wide range universal power supply utilizing a switching regulator (see block diagram in Figure 1).

1.1 AC input

AC input consists of AC inlet, EMI filter (C901~C903, C906~C909) and rectifier D901. Rectifier circuits adapt to full-wave method.Inrush current limiting circuit (R901) protects from excessive inrush current at initial stage of power on.

1.2 Circuit #1 :

Circuit 1 consists of chopper inductor (L910), chopper component (Q910),rectifier component (D910,C911) and control IC (I911). R911,R912 andR913 detect input voltage and provide signal to I911 pin 3 which adjusts the pulse width based on the pin 3 voltage level to provide constant voltage output. Switching operation is performed by frequency synchronization with circuit #2, to control I911 pin 14 from circuit #2.

1.3 Switching Regulator circuit

Switching Regulator circuit is designed to handle variations of two conditions to ensure constant +B voltage to secondary circuit : (Circuit 2) varying load conditions of video, (Circuit 3) varying horizontal frequencies and varying load conditions.

1.3.1 Circuit #2 :

Circuit 2 consists of chopper transformer (T930), chopper component (Q930) and control IC (I931). T930 detects output voltage and provides signal to I931 pin 1 which adjusts the pulse width based on the pin 1 voltage level to provide constant voltage output. If the secondary circuit becomes overloaded, primary current through T930 is detected at R931, R932 and stops the switching operation. Once the circuit has overloaded, the power switch must be turned off for a short period and then turned on to re-establish power.
Switching frequency is determined by time constant of C934.

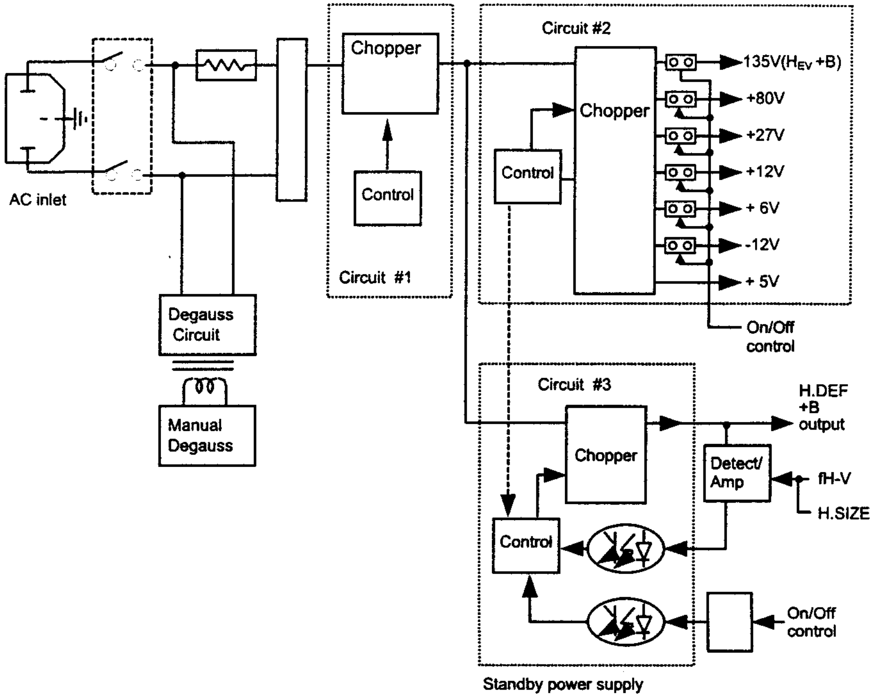
1.3.2 Circuit #3 :

Circuit 3 consists of chopper transformer (T920) and chopper component (Q920) mainly providing +B voltage for horizontal deflection. Regulator method is to detect secondary voltage at I971 and feed through photocoupler I923, providing constant voltage by controlling I921 pin 2 at primary circuit. Switching operation is performed by frequency synchronization with circuit #2, to control I921 pin 7 from circuit #2.
As mentioned above, while detecting secondary voltage at I971. I971 simultaneously receives voltage information from microprocessor which is proportional to the horizontal frequency. Therefore, output of circuit #3 is additionally regulated by the horizontal frequency. In this circuit, gate circuit (Q972, Q973) controls the switching operation at power control (I921) through photocoupler (I922).
This circuit is designed to receive power off command from the microprocessor, resulting in stopping chopper operation at the power supply.

1.4 Degaussing circuit

When the power is switched on, the CRT is degaussed automatically by current flowing through the degauss circuit while the relay (S91R) is closed. Degaussing current flows for approximately 20 seconds and stops after secondary circuit operation is stabilized causing relay (S91R) to be opened.
The circuit also allows for manual degauss by user switch at front panel which closes S91R through Q999, to allow current to flow through the degauss coil.

Figure 1 : Block diagram for power supply circuit



2. Sync Determination Circuit

Depending on the combination of Sync signal inputs and its polarity, Sync signal is fed to Sync Processing chip I304 which produces H/V sync. sep at its output.

3. Video Processing Circuit

3.1 Video Processor

The video input signal of 0.7 Vp-p is amplified to approximately 50 Vp-p by the video processing circuit and is fed to the cathode to drive the beam current.
This chassis incorporates a single chip video processor, I201, with three channels, one for each of R/G/B, which functions as the pre-amp of the inputs, OSD mixer and also gain control. A control signal from the microprocessor changes the amplifier gain of the video channels (R/G/B) together with white balance control. Video Output circuit I202 amplifies R/G/B signals controlled by I201 to the enough level to drive Cathode of CRT. DC voltage of Cathode is determined by DC Cut off voltage from Cathode Clamp Circuit. DC Cut off voltage is generated at Level Shift Circuit which consists of I203, whose R/G/B channels are also controlled by microprocessor.

3.2 ACL Circuit

The current at the secondary winding of the flyback transformer is used to represent the CRT beam current. The current is measured and fed to the contrast control I204, D273 to limit the maximum beam current with negative feedback.

3.3 Blanking Circuit

Video blanking during the beam retrace period is achieved by applying both horizontal and vertical blanking pulses to I201.

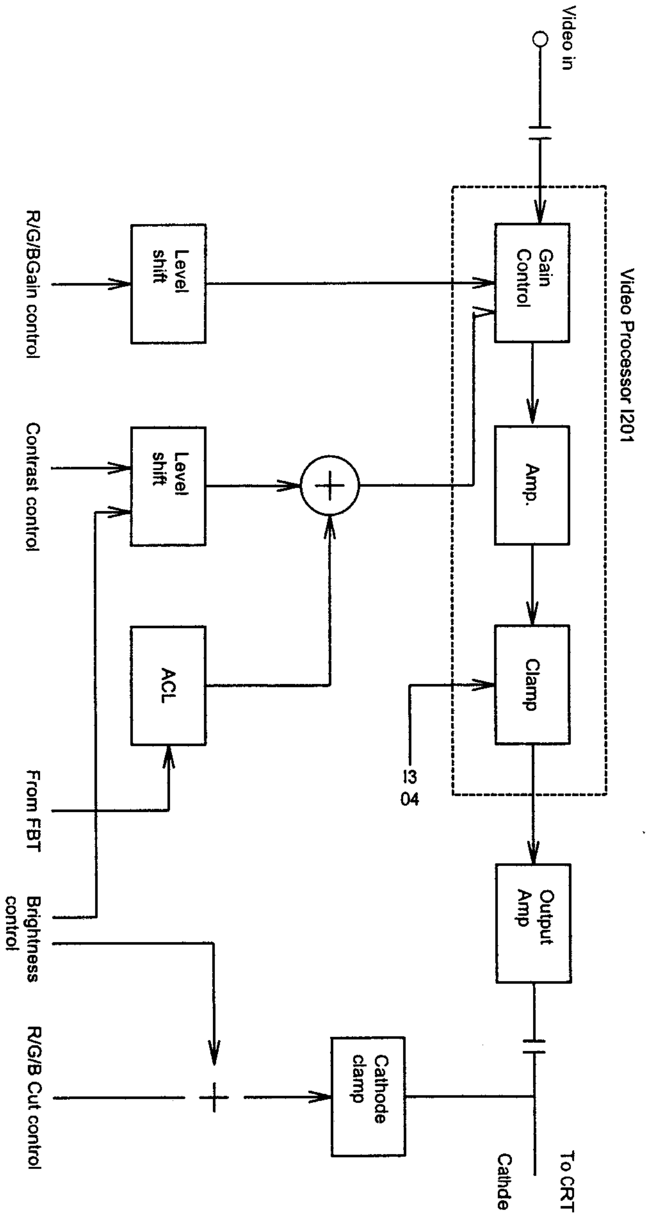
3.4 Precedence of Clamp Pulse Circuit

Clamp signal in Video Processor I201 receives pulses from I306, Precedence of Clamp pulse circuit. When the monitor receives signals, the input of I306 is Sync pulse from Sync Processing Circuit, I304. Without signals, I306' input is the pulse from Deflection Circuit controlled by microprocessor.

3.5 OSD Circuit

I301, receives H/V pulses from Deflection Circuit and control signal from microprocessor, whose output feeds Clock signals (20MHz ~ 90MHz) synchronized with H pulse and control signals from microprocessor, whose output feeds OSD display signals in R/G/B and OSD blanking signal to OSD Mixer Circuit in I201.

Video Process Circuit



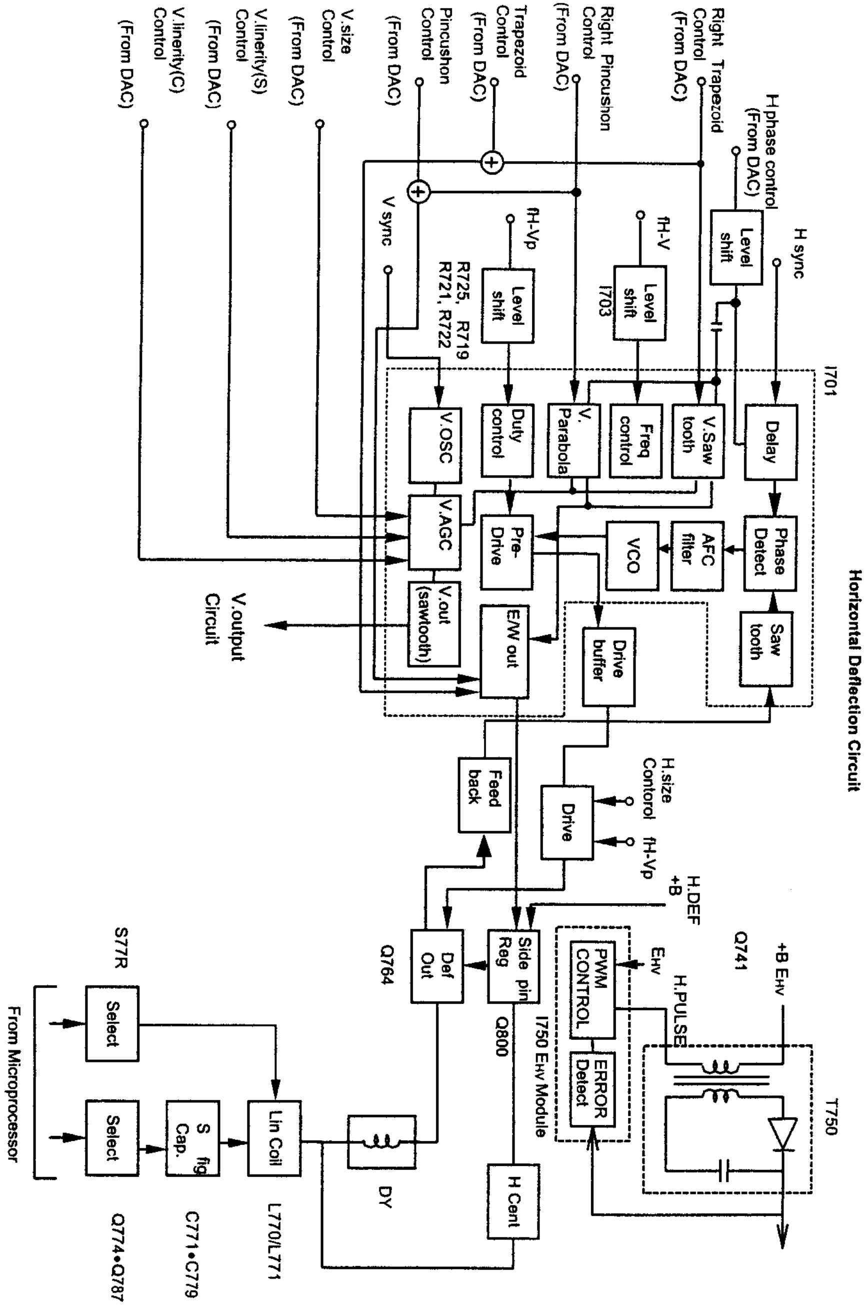
4. Horizontal Deflection and High Voltage Regulation Circuit

4.1 Horizontal Deflection Circuit

The purpose of the horizontal deflection circuit is to cause the CRT electron beam to be scanned horizontally by driving a current through the deflection yoke, synchronized by the H sync pulse. The circuit consists of an AFC circuit, made up of an H phase detector and VCO (voltage controlled oscillator), and the deflection output.
The H.sync signal is input to I701 where it is delayed and then input to a phase detector.The phase detector (I701) also accepts input from a sawtooth waveform which is provided by the deflection feedback (flyback pulse) through the Q704.The output of the phase detector creates an error voltage between the feedback pulse and the input pulse and is then fed to the VCO after processing by an AFC Filter.
The AFC circuit also receives controller voltage from the microprocessor' s output of the f_{H-V} signal, to center the free-run frequency within the pull-in range of 31~130kHz, achieving a wide pull-in range. The output pulse from the VCO is fed to the pre-drive and then output from I701 to the drive buffer Q701/Q702. The pre-drive circuit within I701 is duty cycle controlled by the f_{H-VP} signal from the microprocessor through a level shifter R719, R721, R722 and R725.
In the case of no Sync signals supplied or excessive frequency change, such as a signal timing change, the microprocessor provides a +B shutdown signal to the power supply and also provides a control signal which determines the +B shutdown period after receiving an input signal again.
The deflection circuit of the DJ81 chassis has been separated from the high voltage regulation circuit to provide improved H linearity performance by utilizing the consonant conditions of the horizontal beam current characteristics. The S-consonant capacitors, C771~C779, are changed by Q774~Q787, which provide 12~10 stages of consonant conditions. The horizontal linearity coils L770~L771 are changed by S77R to provide two stages of H Linearity conditions.
The power supply parabolically modulates the H.DEF +B voltage of the deflection circuit, based on the horizontal frequency, to provide a frequency - dependent voltage of between 53.5V and 174V to the deflection circuit.

4.2 High Voltage Regulation Circuit

The output pulse from I504 is also fed to the high voltage regulation circuit with the same design of consonant circuit as the horizontal deflection circuit. High voltage of 27.5kV is obtained by the step-up windings of the flyback transformer to drive the CRT anode. The high voltage is monitored by the E_{HV} error detection circuit. The error detection circuit functions by stepping the high voltage down and comparing it with the reference voltage of inside I750 whose output controls Q741, the E_{HV} switching transistor.


Right Trapezoid Control (From DAC)
Right Pincushon Control (From DAC)
Trapezoid Control (From DAC)
Pincushon Control (From DAC)
V.size Control (From DAC)
V.linerity(S) Control (From DAC)
V.linerity(C) Control (From DAC)
H phase control (From DAC)
H sync
fH-V
fH-Vp
V sync
Level shift
Level shift
I703
Level shift
R725, R719
R721, R722
I701
Delay
V.Saw tooth
Freq control
V. Parabola
Duty control
V.OSC
Phase Detect
AFC filter
VCO
Pre-Drive
V.AGC
Saw tooth
Drive buffer
E/W out
V.out (sawtooth)
V.output Circuit
Feed back
Drive
H.size Contorol
fH-Vp
H.DEF +B
+B EHV
Q741
EHV
H.PULSE
PWM CONTROL
ERROR Detect
I750 EHV Module
T750
Side pin Reg
Q800
Def Out
Q764
H Cent
DY
Lin Coil
L770/L771
S fig Cap.
C771•C779
Select
Select
S77R
Q774•Q787
From Microprocessor

Horizontal Deflection Circuit

4.3 Parabolic Waveform Generator Circuit

This circuit generates the parabolic waveform for the purpose of dynamic focus compensation.

4.4 Dynamic focus compensation waveform

Vertical saw tooth signal are input to I505 pin2. Output of pin 4 generates a parabolic waveform with an amplitude proportional to the vertical line frequency, after processing by I505. Vertical parabolic waveform output (I505 pin 4) pulse to feed to the dynamic focus drive circuit.
Horizontal trigger pulses are input to the PLL (I503, pin 14), the stabilized output of which is then fed to I505 pin 17, through Gate I504. The output of I505 (pin 7) feeds the parabolic waveform, with an amplitude proportional to the horizontal line frequency (after processing by I505), to I501. I501 is a processor which combines horizontal parabolic output pulse to feed to the dynamic focus drive circuit.

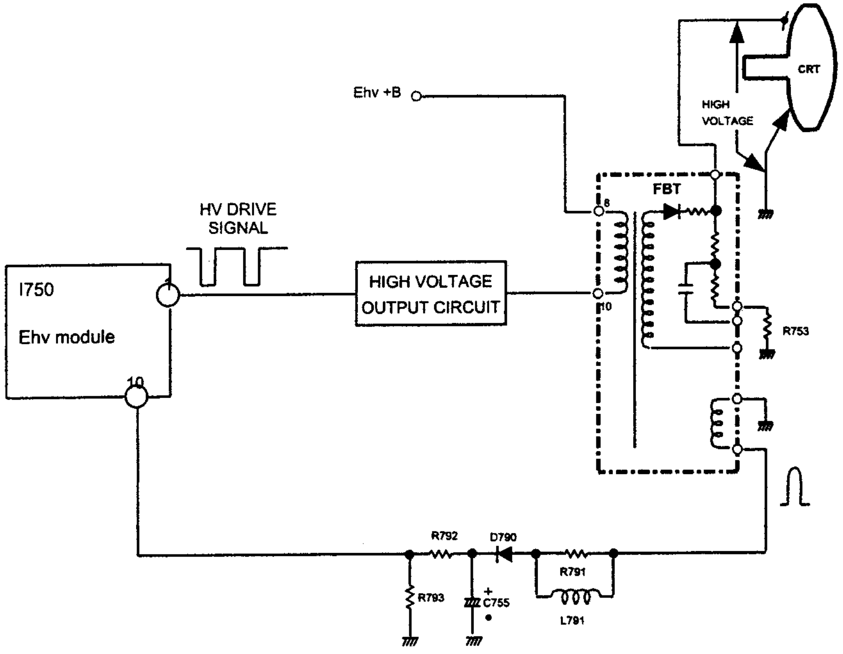
4.5 Dynamic focus drive circuit

This monitor' s CRT includes a dynamic focusing electron gun to achieve sharp and uniform focus throughout the display area. The CRT's Focus anode receives a DC component of approximately 27% of the CRT anode voltage, combined with the AC voltage parabolic waveform of magnitude of 550Vp-p horizontal, and 200Vp-p vertical. DC focus voltage is obtained from a tap of the flyback transformer's bleeder resister, and fed to G3 focus electrode. Horizontal and vertical parabolic output pulses are amplified at Q560~Q564,T560 and fed to the flyback transformer where they are combined with the DC component (27% of anode voltage). The potentiometers (focus 1, focus 2) at the flyback adjust the DC focus voltage. The focus 1 potentiometer mainly adjusts horizontal beam shape (vertical line width), and the focus 2 potentiometer mainly adjusts the vertical beam shape (horizontal line width) by optimizing the DC component of the parabolic waveform.
Left and right horizontal focus adjustment is achieved by changing the amplitude of the horizontal parabolic waveform at I505 via horizontal gain at R544. Top and bottom vertical focus adjustment is achieved by changing the amplitude of the vertical parabolic waveform via vertical gain at R543.

4.6 High Voltage Hold-Down Circuit

DJ81- Chassis uses a system that to stop HV DRIVE SIGNAL output,when abnormal high voltage is detected.
So that the high voltage output will be declined to zero. The circuit operation in detail is as follows.
When an input voltage to I750 (pin10,it is determined by R792 and R793) exceeds the specified level HV DRIVE SIGNAL is not output in order to prevent over drive. This cause the high voltage to decline to zero.

HIGH VOLTAGE HOLD-DOWN CIRCUIT DIAGRAM



5. Vertical Deflection Circuit

The purpose of the vertical deflection circuit is to cause the CRT electron beam to be scanned vertically by driving a current through the deflection yoke, synchronized by the V sync pulse. V sync is input to the V oscillator circuit, I701, generating the vertical sawtooth wave. The vertical sawtooth wave is fed to I630 to be amplified of I630 to drive the vertical deflection yoke.

The vertical output stage consist of a DC feed back loop, with feedback of the DC component via the low pass filter, and an AC feedback loop with feedback of the AC component. The AC feedback current gose through feedback circuit where it is used to adjust the time constant.

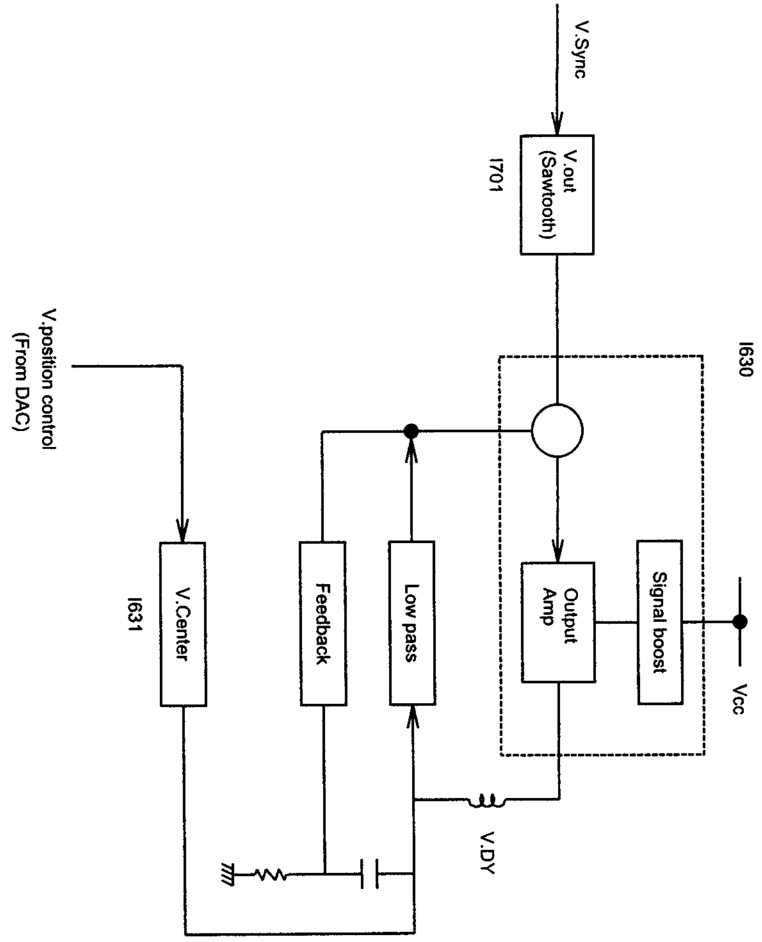
The vertical linerity after signal timing change is constant by fv-v voltage whitch is from microprcessor circuit.

The vertical size control signal from the microprocessor controls the voltage of I701 8pin through a level shifter R618,R619 and R606.

The output stage of I630 includes a ramp-up circuit with D630 and C635 achieving near doubling of the retrace pulse to minimize retrace time.

The vertical position control signal from the microprocessor is fed to the vertical deflection yoke through a vertical centering circuit of I631 to center the raster.

Vertical Deflection Circuit



6. Microprocessor Circuit

The microprocessor circuit consists of the following four detailed circuits as shown in Figure.

1. Sync detect circuit
2. Front panel key data Input / Output (I/O)
3. Processing and memory
4. Control output

6.1 Sync detect circuit

The sync detect outside the microprocessor determines sync polarity, and feeds the polarity signal, STATE signal and H/V sync to the sync processing circuit within the microprocessor. The sync processing circuit detects these inputs, counts frequency, and feeds the polarity signal and frequency count to the Central Processing Unit (CPU).

6.2 Front panel key data Input / Output (I/O)

User input is received by the front panel keys which consists of : six select keys, four data keys (two pairs of +/- key), one Store key.

Select keys:

1)	H. Position / H. Size	4)	Right Side Pin / Right Trapezoid
2)	V. Position / V. Size	5)	Color Select / Rotation
3)	Side Pin / Trapezoid	6)	Contrast / Brightness

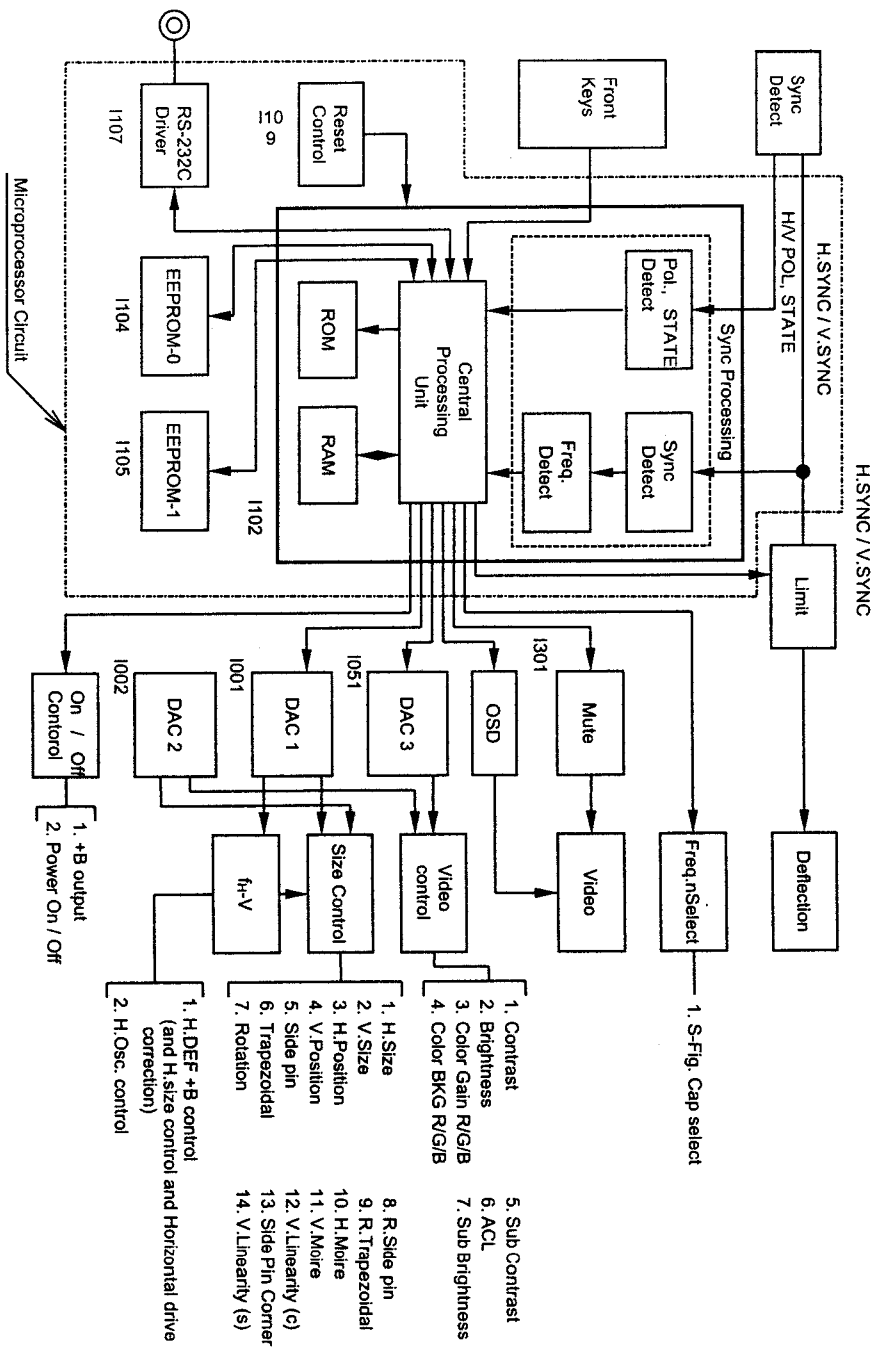
The H.moire control feature requires the user to press Right Side Pin / Right Trapezoid and Contrast / Brightness front panel keys simultaneously to enter the control mode. Adjustment is then made with +/- keys.
The V.moire control feature requires the user to press Color Select / Rotation and Contrast / Brightness front panel keys simultaneously to enter the control mode. Adjustment is then made with +/- keys.
Red, Green, and Blue color gain control feature requires that the user press the contrast / Brightness button and one of H. Position / H. Size (Red adjust), V. Position / V. Size (Green adjust), or side Pin / Trapezoid (Blue adjust) keys simultaneously to enter the control mode. Adjustment for the selected color is then made with +/- keys.
The language select feature requires the user to press V.Position / V.Size and Side Pin / Trapezoid front panel keys simultaneously to enter the control mode. Adjustment is then made with +/- keys.
When OSD display is disappeared, current settings (including picture size, geometry, and color setting) were stored to non-volatile memory. The maximum memory capacity is for 26 presets including factory standard settings.

6.3 Processing and memory

I102 is an 8 bit microprocessor which equips with ROM and RAM for system program, and sync processing circuit. Data memory consists of 2 EEPROM chips, I104, I105 for preset data.

6.4 Control output

The microprocessor output controls the DAC, the OSD On/Off controls, mute circuit, and limit circuit. The input control signal to the DAC, I001, I002 I051, is fed to video control (Contrast, Brightness, R/G/B color gain, R/G/B color BKG, sub Contrast, Sub Brightness and ACL), Size control (H/V size, H/V position, side pin correction, trapezoidal correction, rotation, right sidepin correction, right trapezoidal correction, H/V moire control, V.Linearity(S), V.Linearity(C) and Side pin Corner correction), and fH-V selection (+B control and H size control and horizontal drive correction, H. Osc. control with VCO control). The input control signal to the OSD,I301,provides the function that the monitor shows guidance for adjustment on the screen by generating video signal as character pattern and feeding it to the video amplifier. On/Off control provides 2 power saving modes by stopping +B output if one of H sync and V sync is not supplied (Standby mode) and by stopping main power supply if both H and V sync are not supplied. The mute circuit brings video output to black level when timing signal changes or the monitor goes into the power saving mode. The limit circuit consists of a gate, I704 and I706. In case that the frequency is normal, CPU opens the gate and H/V sync is fed to the deflection circuit via the gate. If not, CPU closes the gate to prevent the deflection circuit oscillating at illegal frequency.
This chassis is capable of communicating with a PC through an RS-232C serial communication port for factory adjustments, by making access to the microprocessor through the RS-232C I/O driver, I107.


Microprocessor Circuit
RS-232C Driver
I107
Reset Control
I109
Front Keys
Sync Detect
EEPROM-0
I104
EEPROM-1
I105
ROM
RAM
Central Processing Unit
I102
Pol., STATE Detect
Sync Processing
Freq. Detect
Sync Detect
H/V POL, STATE
H.SYNC / V.SYNC
H.SYNC / V.SYNC
Limit
Deflection
On / Off Contorol
I002
DAC 2
I001
DAC 1
I051
DAC 3
OSD
I301
Mute
fH-V
Size Control
Video control
Video
Freq.nSelect
1. +B output
2. Power On / Off
1. H.DEF +B control (and H.size control and Horizontal drive correction)
2. H.Osc. control
1. H.Size
2. V.Size
3. H.Position
4. V.Position
5. Side pin
6. Trapezoidal
7. Rotation
8. R.Side pin
9. R.Trapezoidal
10. H.Moire
11. V.Moire
12. V.Linearity (c)
13. Side Pin Corner
14. V.Linearity (s)
1. Contrast
2. Brightness
3. Color Gain R/G/B
4. Color BKG R/G/B
5. Sub Contrast
6. ACL
7. Sub Brightness
1. S-Fig. Cap select

7. Power Save Function

The C98 chassis is capable of power savings by sensing of the sync input conditions by the microprocessor. The microprocessor can identify two sync conditions, (1) No detection of H.sync, (2) No detection of V sync. The following table shows the details of the Power save mode.

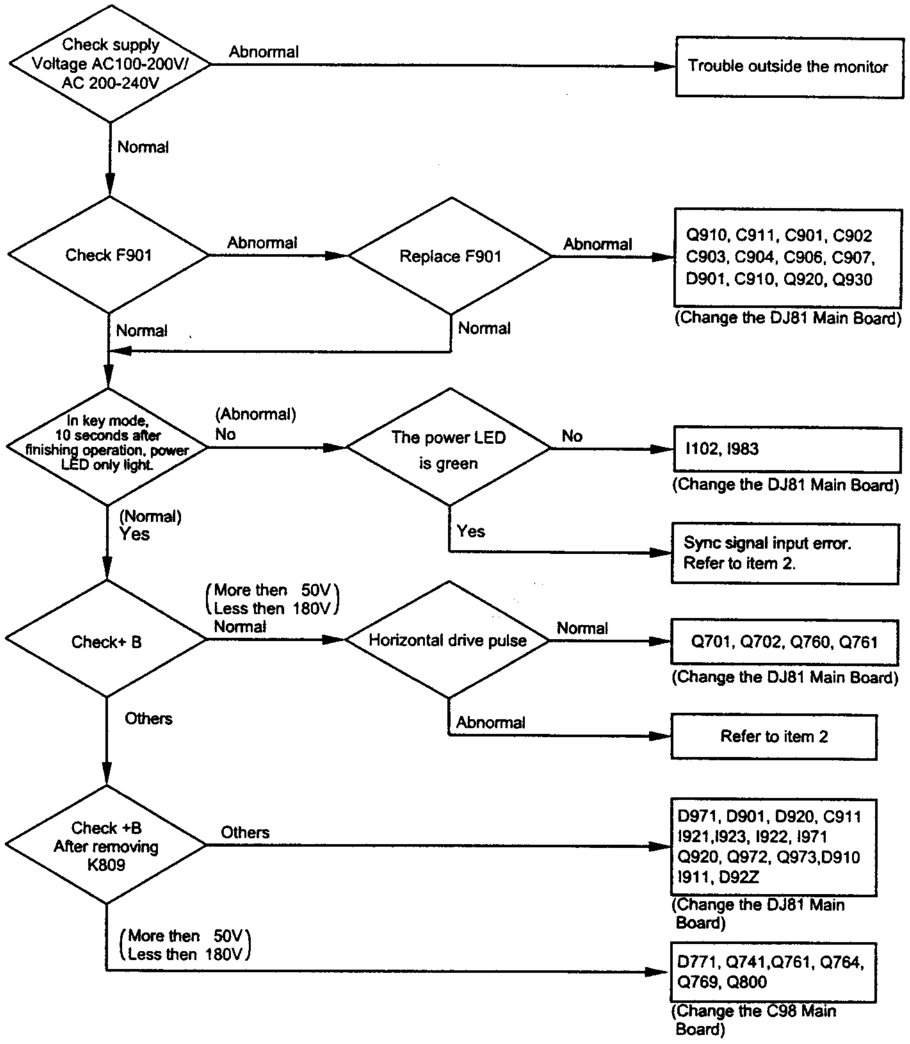
Table: Power Save Function

Sync	H Sync	Yes	No	Yes	No
	V Sync	Yes	Yes	No	No
VESA Standard	Name	Normal	Standby	Suspend	Off
	Recovery Time	N/A	Short	Short	System Dependent
	Recovery Time	None	Minimum	Minimum	Maximum
Circuit Operation	H. Deflection	Normal operation	Stop	Stop	Stop
	V. Deflection	Normal operation	Stop	Stop	Stop
	Video	Normal operation	Mute	Mute	Mute
Power LED		Lighting Green	Flashing quickly	Flashing quickly	Flashing slowly
Power consumption (Typical) : AC (120V)		All White : 125W All Black : 90W	less than 15W	less than 15W	less than 5W

TROUBLESHOOTING

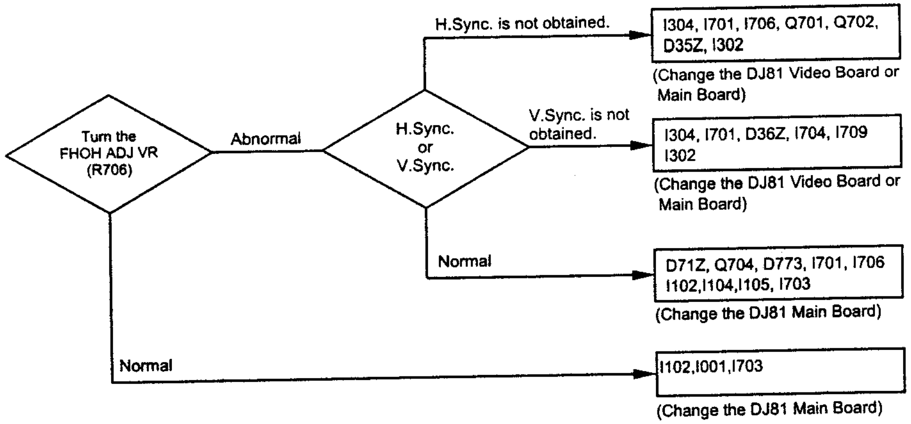
1. RASTER DOES NOT APPEAR

Relevant circuit : Power circuit, Horizontal deflection circuit,
High voltage limitter circuit


Check supply Voltage AC100-200V/ AC 200-240V
Abnormal
Trouble outside the monitor
Normal
Check F901
Abnormal
Replace F901
Abnormal
Q910, C911, C901, C902 C903, C904, C906, C907, D901, C910, Q920, Q930
(Change the DJ81 Main Board)
Normal
Normal
In key mode, 10 seconds after finishing operation, power LED only light.
(Abnormal) No
The power LED is green
No
I102, I983
(Change the DJ81 Main Board)
(Normal) Yes
Yes
Sync signal input error. Refer to item 2.
Check+ B
(More then 50V Less then 180V) Normal
Horizontal drive pulse
Normal
Q701, Q702, Q760, Q761
(Change the DJ81 Main Board)
Others
Abnormal
Refer to item 2
Check +B After removing K809
Others
D971, D901, D920, C911 I921,I923, I922, I971 Q920, Q972, Q973,D910 I911, D92Z
(Change the DJ81 Main Board)
(More then 50V Less then 180V)
D771, Q741,Q761, Q764, Q769, Q800
(Change the C98 Main Board)

2. SYNVHRONIZATION IS NOT OBTAINED

Relevant circuit : Sync. input circuit, Deflection circuit


Turn the FHOH ADJ VR (R706)
Abnormal
H.Sync. or V.Sync.
H.Sync. is not obtained.
I304, I701, I706, Q701, Q702, D35Z, I302
(Change the DJ81 Video Board or Main Board)
V.Sync. is not obtained.
I304, I701, D36Z, I704, I709 I302
(Change the DJ81 Video Board or Main Board)
Normal
D71Z, Q704, D773, I701, I706 I102,I104,I105, I703
(Change the DJ81 Main Board)
Normal
I102,I001,I703
(Change the DJ81 Main Board)

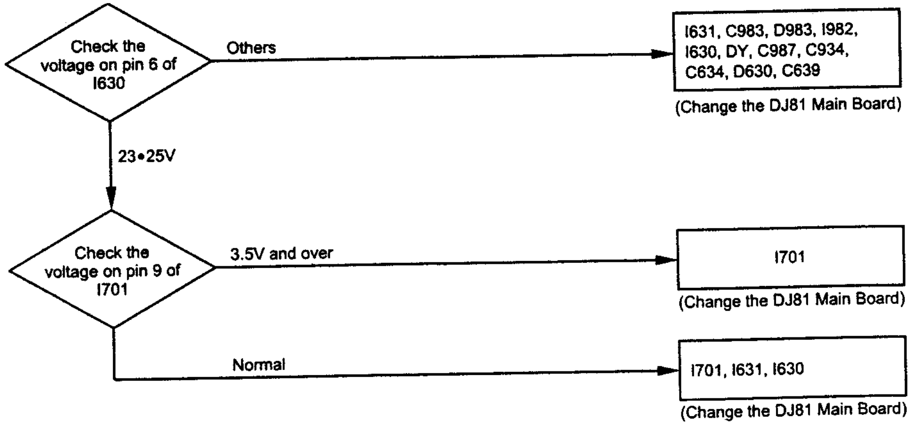
3. HORIZONTAL SINGLE LINE

Relevant circuit : Horizontal output circuit

DY faulty, Q800, D771, Q764, Q760

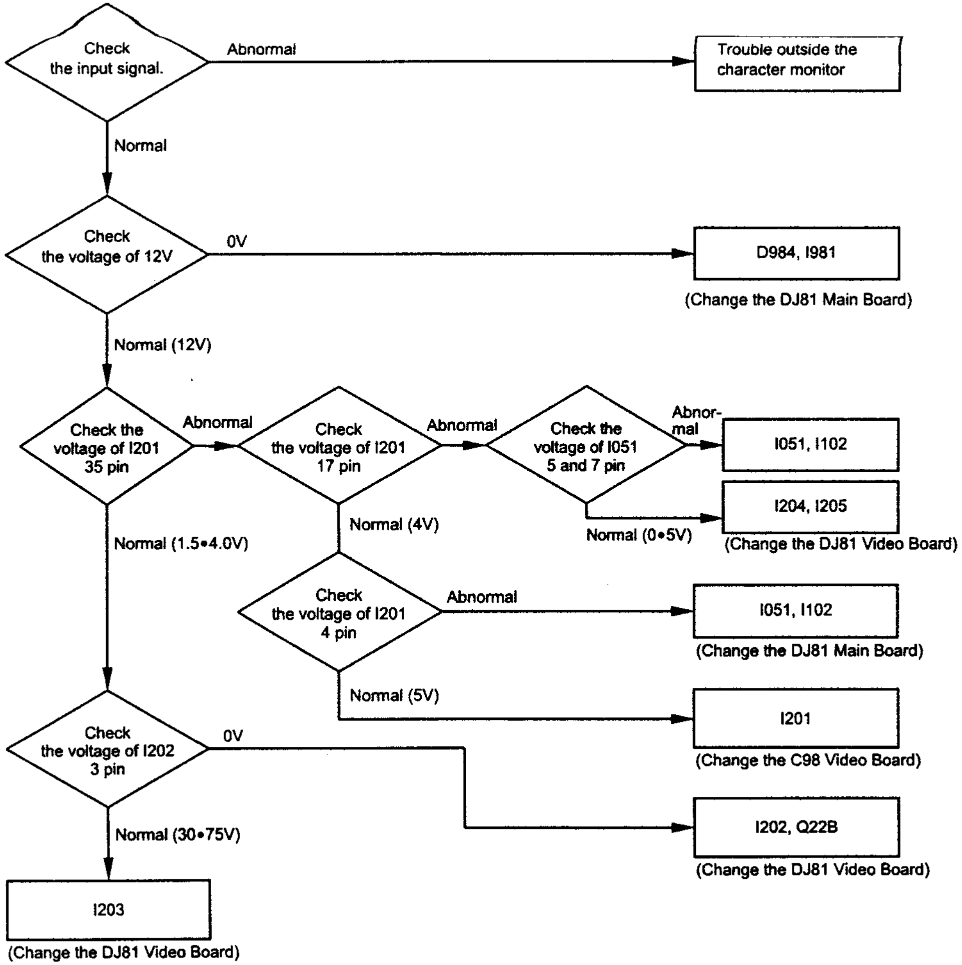
4. VERTICAL SINGLE LINE

Relevant circuit : Vertical deflection circuit


Check the voltage on pin 6 of I630
Others
I631, C983, D983, I982, I630, DY, C987, C934, C634, D630, C639
(Change the DJ81 Main Board)
23•25V
Check the voltage on pin 9 of I701
3.5V and over
I701
(Change the DJ81 Main Board)
Normal
I701, I631, I630
(Change the DJ81 Main Board)

5. COLOR DOES NOT APPEAR

Relevant circuit : Video amplifier circuit


Check the input signal.
Abnormal
Trouble outside the character monitor
Normal
Check the voltage of 12V
0V
D984, I981
(Change the DJ81 Main Board)
Normal (12V)
Check the voltage of I201 35 pin
Abnormal
Check the voltage of I201 17 pin
Abnormal
Check the voltage of I051 5 and 7 pin
Abnor-mal
I051, I102
Normal (0•5V)
I204, I205
(Change the DJ81 Video Board)
Normal (4V)
Check the voltage of I201 4 pin
Abnormal
I051, I102
(Change the DJ81 Main Board)
Normal (5V)
I201
(Change the C98 Video Board)
Normal (1.5•4.0V)
Check the voltage of I202 3 pin
0V
I202, Q22B
(Change the DJ81 Video Board)
Normal (30•75V)
I203
(Change the DJ81 Video Board)

Note : Trouble in the blue circuit is shown in this diagram as representative color.
Refer to : when green does not appear, and when red does not appear.

ADJUSTMENTS

1. Power supply

1.1 PFC output voltage adjustment.

(1) Turn the switch of the unit off.
(2) Place a jumper wire across C922 and R98P on main-p.w.b to disable + B output voltage.
(3) Turn the switch of the unit on.
(4) Receive normal cross hatch pattern of signal 94A.
(5) Connect a Digital multimeter between + and - of C911.
(6) Adjust R916 to 373 ± 2V.
(7) Turn the switch of the unit off.
(8) Remove the jumper wire from C922 and R98P.

1.2 Main power supply voltage adjustment for color display tube.

(1) Turn the switch of the unit off.
(2) Place a jumper wire across C922 and R98P on main-p.w.b to disable + B output voltage.
(3) Turn the switch of the unit on.
(4) Receive reverse cross hatch pattern of signal 94A.
(5) Connect a Digital multimeter across C984.
(6) Adjust Main power supply voltage to 13.0 ± 0.3V using R942.
(7) Turn the switch of the unit off.
(8) Remove the jumper wire from C922 and R98P.

1.3 +B voltage adjustment

(1) Turn the switch of the unit off.
(2) Adjusting horizontal free running frequency must be finished before this adjustment.
(3) Receive a normal cross hatch signal.(See table 1.for proper signal timing)
(4) Connect a Digital volt meter across C971.
(5) Turn the switch of the unit on.
(6) Adjust H.Size to maximum.
(7) Adjust R973 to the proper +B voltage value as outlined in table 1.
(8) Receive reverse cross hatch pattern of signal 30C and check the +B voltage is at 50.0 ± 2.0V.

Table 1

Model	signal	+B voltage
CM81*	94A	135±1.0V

2. Deflection circuit adjustment

2.1 Horizontal free running frequency and Horizontal drive pluse duty adjustment

(1) Turn the switch of the unit off.
(2) Place a jumper wire across C922 and R98P on main-p.w.b to disable +B output voltage.
(3) Connect a 1 Kohm resister between R700 (Q701 side) and D71Z's cathode.
(4) Place a jumpwer wire between I701 26pin and GND.
(5) Connect frequency counter between R700 (Q701 side) and GND.
(6) Turn the switch of the unit on.
(7) Receive the signal, as indicate on table 2, for frequency Horizontal high(fHH), and adjust R706 to the value indicated on table 2.
(8) Receive the signal 30W for fHLL and check the fHOL in table 2.
(9) Connect a oscilloscope's probe (10:1) to Q760's drain.
(10) Ajust tHD to table 2 using R725
(11) Turn the switch of the unit off .
(12) Remove the adjustment jig.

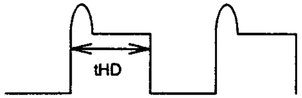


Table 2

			R725		R706	
	fHLL	fHOL	fHLL	tHD	fHH	fHOH
CM81*	30W	30.0±0.7kHz	30W	16.6±0.2•s	94A	93.75±0.1kHz

2.2 High voltage adjustment

(1) Turn the switch of the unit off.
(2) Connect a high voltage meter, whitch is capable to measure up to 40kV, between CDT anode and GND.
(3) Receive normal cross hatch pattern of 94A signal.
(4) Turn the switch of the unit on.
(5) Adjust high voltage level to 27.5 ± 0.3kV using R754.
(6) Turn the switch of the unit off.
(7) Remove the adjustment jig.

3. Video Circuit

Prior to the video circuit adjustment, all Sync.And Deflection circuit adjustment must be completed. The monitor must have been warmed up for more than 60 minutes. Video signal must be terminated with 75ohm and should provide the correct voltage at the monitor end.

[Pre-setting before adjustment]

Function	Pin No.	Output Voltage
R Color	#9 pin (I051)	5V (FF)
G Color	#6 pin (I051)	5V (FF)
B.Color	#8 pin (I051)	5V (FF)
Contrast	#7 pin (I051)	5V (FF)
Brightness	#4 pin (I051)	0V (FF)
Sub Brightness	#8 pin (I002)	2.5V (7F)
Sub Contrast	#5 pin (I051)	2.5V (7F)
R.BKG	#15 pin (I051)	5V (00)
G.BKG	#14 pin (I051)	2.5V (7F)
B.BKG	#16 pin (I051)	5V (00)
ACL	#17 pin (I051)	2.5V (7F)

* Output voltages of DAC

Note: 1) Color Analyzer : Minolta CA 100 or equivalent.

3.1 Cut off adjustment

(1) Receive a signal of 94A with a blank signal pattem.(Black video)

(2) Connect a high impedance voltmeter (more than 1000MΩ) to the Screen terminal (G2) on the CRT neck board.
Adjust the Screen voltage pot on FBT to see 600 ± 5V.

(3) Adjust R,G & B,BKG to show the CIE coordinate of:
X=0.313±0.03, Y=0.329±0.03 at 1.5 cd/m^2 (0.44ft-L).
If it looks difficult to obtain X and Y readings mentioned above, do the followings to obtain these numbers.
  1) Reset Sub Brightness to 1.9V (9F) or 3.1V (60).
  2) Reset Sub Brightness to 0.93V (CF) or 4.1V (30).
  3) Reset G2 to 550V or 650V

3.2 White balance adjustment (Color 2)

(1) Receive a signal of 94A with a 100x100mm window pattern.
(2) Set Brightness Control to the center (2.5V : 7F).
(3) Adjust the light output to 80 cd/m^2(23ft-L) at the center of screen by adjusting Sub Contrast Control.
(4) Adjust the white balance of high light output by Green and Blue color adjustments to read CIE coordinate of X=0.313 ± 0.008, Y=0.329 ± 0.008.
(5) Adjust Contrast Control to read 3 cd/m^2 (1 ft-L).
(6) Adjust Red and Blue BKG to read the same CIE coordinate shown in 3.2.(4)
(7) Adjust Contrast Control to read 80 cd/m^2(23ft-L) and then confirm CIE coordinate. If it shown out range, go back to 3.2(4)
(8) Register the readings of R/G/B BKG and Color data (Color 2) to the microprocessor.

3.3 White balance adjustment (Color 1)

(1) Receive a signal of 94A with a 100×100mm window pattern.
(2) Set brightness Control to the center (2.5V : 7F).
(3) Adjust the light output to 80 cd/m^2(23ft-L) at the center of screen by adjusting Sub Contrast Control in Color 2 mode.
(4) Select ''Color Select'' to Color 1.
(5) Adjust the white balance of high light output by Green and Blue color adjustments to read CIE coordinate of X=0.283 ± 0.008, Y=0.298 ± 0.008
(6) Register the readings of Color data (Color 1) to the microprocessor.

3.4 White balance adjustment (Color 3)

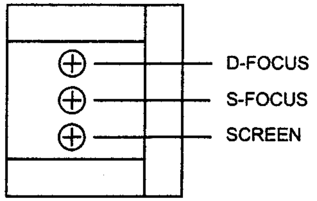
(1) Receive a signal of 94A with a 100×100mm window pattem.
(2) Set Brightness Control to the center (2.5V : 7F).
(3) Adjust the light output to 80 cd/m^2 (23ft-L) at the center of screen by adjusting Sub Contrast Control in Color 2 mode.
(4) Select ''Color Select'' to color 3.
(5) Set Red color to the maximum (5V ; FF).
(6) Adjust the white balance of high light output by Green and Blue color adjustments to read CIE coordinate of X=0.336 ±0.008, Y=0.352±0.008.
(7) Register the readings of Color data (Color 3) to the microprocessor.

3.5 Brightness adjustment

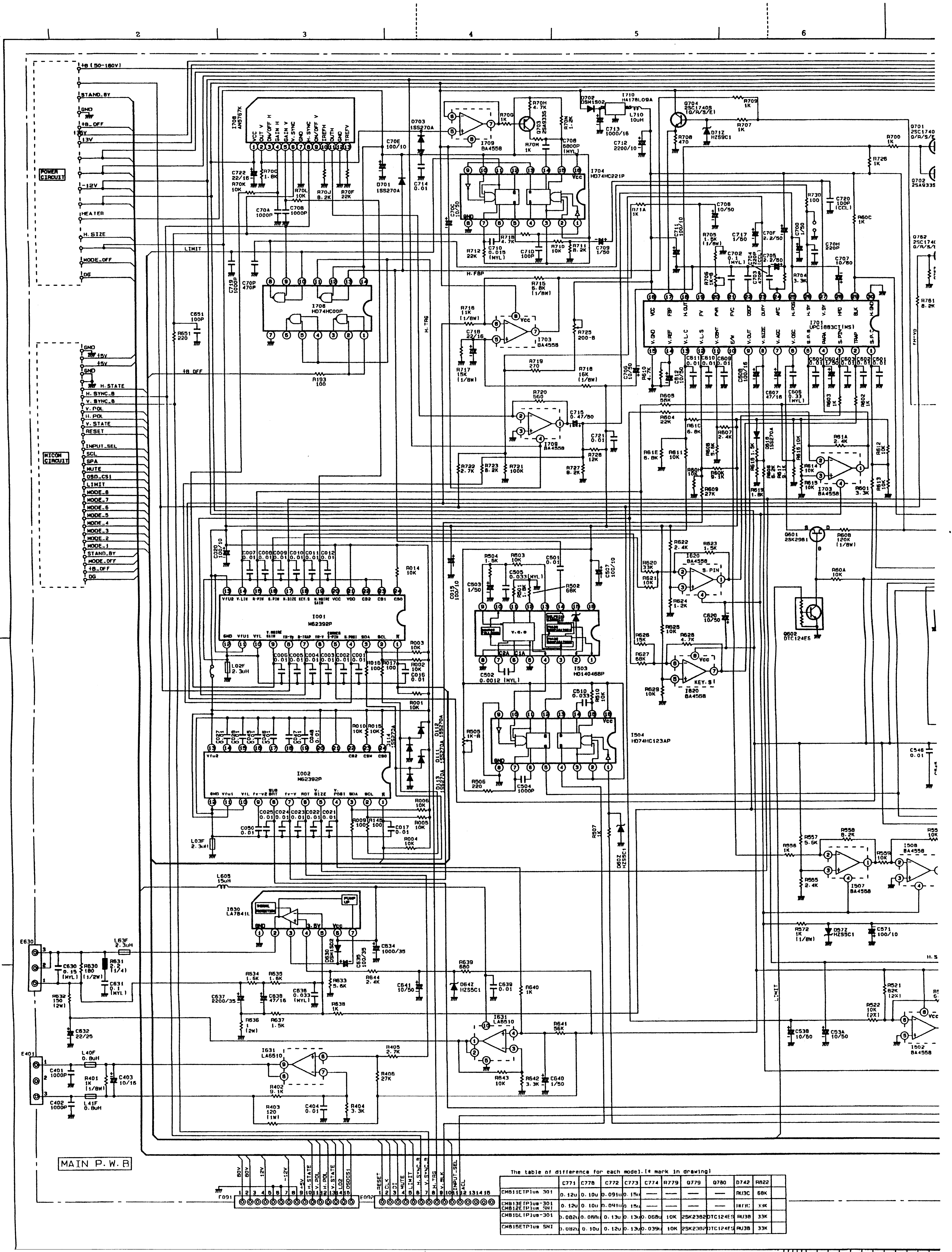
(1) White balance adjustment must have been done before Brightness adjustment.
(2) Receive signal of 94A with a blank signal pattem.(Black video)
(3) Set Brightness and Contrast Control to their maximums.
(4) Ambient light on the surface of the CRT should show lower than 50 lux.
(5) Select ''Color Select'' to Color 1.
(6) Adjust the light output to 1.5 cd/m^2 (0.44 ft-L) at the center of screen by adjusting Sub Brightness Control.
(7) Receive a signal or 94A with a window pattem (100 × 100 mm)
(8) Adjust the light output to 125 cd/m^2 (36 ft-L) at the center of screen by adjusting Sub Contrast Control.
(9) Receive a signal of or 94A with a full white patterm.
(10) Set Video signal level to 0.75V
(11) Adjust the light output to 120 cd/m^2 (35ft-L) at the center of screen by adjusting ACL adjustment.
(12) Register the readings of Sub Brightness, Sub Contrast and ACL to the microprocessor.

4.1 Focus adjustment

(1) Receive signal 94A with a full screen ''E'' characters.
(2) Set user Contrast control to its maximum.
(3) Set user Brightness control so that the back ground raster is just diminished.
(4) Adjust S-Focus control on the FBT so that focus at the middle points between the center of the screen to its best.
(5) Adjust D-Focus control on the FBT so that focus at four corners of the screen to its best.



Position of FBT Controls

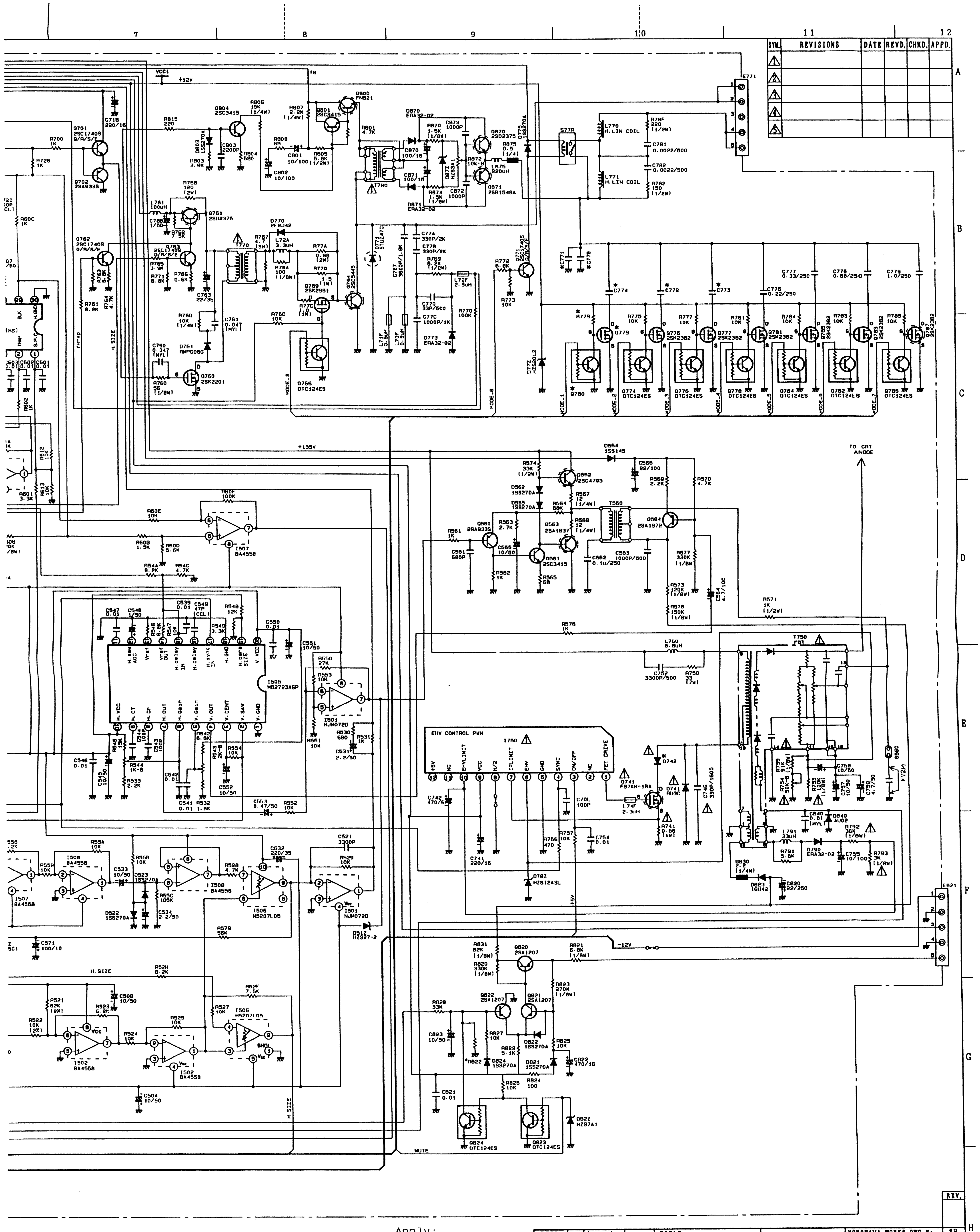

MAIN P.W.B
POWER CIRCUIT
MICON CIRCUIT
I708 AN5767K
I706 HD74HC00P
I704 HD74HC221P
I709 BA4558
I703 BA4558
I701 UPC1883CT(MS)
I001 M62392P
I002 M62392P
I503 HD14046BP
I504 HD74HC123AP
I620 BA4558
I630 LA7841L
I631 LA6510
I507 BA4558
I508 BA4558
I502 BA4558
I710 HA178L09A
Q704 2SC1740S
Q703 2SA933S
Q701 2SC1740
Q702 2SA933S
Q601 2SK2981
Q602 DTC124ES
E630
E401
F001
E002
+B(50-160V)
STAND.BY
GND
+B_OFF
13V
-12V
HEATER
H.SIZE
MODE_OFF
DG
LIMIT
H.STATE
H.SYNC.B
V.SYNC.B
V.POL
H.POL
V.STATE
RESET
INPUT_SEL
SCL
SDA
MUTE
OSD_CS1
MODE_8
MODE_7
MODE_6
MODE_5
MODE_4
MODE_3
MODE_2
MODE_1
H.F8P
H.TAG
S.PIN
KEY.S
1
2
3
4
5
6

The table of difference for each mode].(* mark in drawing)

	C771	C778	C772	C773	C774	R779	Q779	Q780	D742	R822	
CM811ETPlus 301	0.12u	0.10u	0.091u	0.15u	——	——	——	——	RU3C	68K	
CM813ETPlus-301 CM812ETPlus SNI	0.12u	0.10u	0.091u	0.15u	——	——	——	——	RU3C	33K	
CM815LTPlus-301	0.082u	0.068u	0.13u	0.13u	0.068u	10K	2SK2382	DTC124ES	RU3B	33K	
CM815ETPlus SNI	0.082u	0.10u	0.12u	0.13u	0.039u	10K	2SK2382	DTC124ES	RU3B	33K	

ABCDEFGHJKLMNPQRSTUVWXYZ

abcdefghijkmnpqrstuvwxyz


7
8
9
10
11
12
A
B
C
D
E
F
G
H
VCC1
+12V
+B
+135V
Q701 2SC1740S Q/R/S/E
Q702 2SA933S
Q761 2SD2375
Q762 2SC1740S Q/R/S/E
Q763 2SC1740S Q/R/S/E
Q760 2SK2201
Q766 DTC124ES
Q769 2SK2981
Q764 2SC5445
Q800 FN521
Q801 2SC3415
Q804 2SC3415
Q870 2SD2375
Q871 2SB1548A
Q772 2SC1740S Q/R/S/E
T770
T780
D870 ERA32-02
D871 ERA32-02
D872 HZS3A1
D773 ERA32-02
D771 STUZ47C
D770 2FWJ42
D761 RMPG06G
D775 1SS270A
D772 HZS20L2
S77R
L770 H.LIN COIL
L771 H.LIN COIL
E771
Q779
Q775 2SK2382
Q777 2SK2382
Q781 2SK2382
Q785 2SK2382
Q783 2SK2382
Q787 2SK2382
Q780
Q774 DTC124ES
Q776 DTC124ES
Q778 DTC124ES
Q784 DTC124ES
Q782 DTC124ES
Q786 DTC124ES
MODE_1
MODE_2
MODE_3
MODE_4
MODE_5
MODE_6
MODE_7
MODE_8
H.SIZE
fH-VD
TO CRT ANODE
D564 1SS145
Q562 2SC4793
Q560 2SA933S
Q563 2SA1837
Q561 2SC3415
Q564 2SA1972
T560
D562 1SS270A
D565 1SS270A
I507 BA4558
I505 M52723ASP
H.saw AGC
Vref
Vref OUT
H.delay IN
H.delay
H.sync IN
H.GND
H.para SIZE
V.VCC
H.VCC
H.CT
H.Cr
H.OUT
H.Gain
V.Gain
V.OUT
V.CENT
V.SAW
V.GND
I801 NJM0720
L760 5.6uH
T750 FBT
EHV CONTROL PWM
I750
+5V
NC
EHVLIMIT
VCC
H/2
IPLIMIT
EHV
GND
SYNC
ON/OFF
FET DRIVE
Q741 FS7KM-18A
D741 RU3C
D742
D782 HZS12A3L
L74F 2.3uH
L791 33uH
D790 ERA32-02
D823 1GU42
D840 AU02
E821
I508 BA4558
I506 M5207L05
I501 NJM0720
D522 1SS270A
D523 1SS270A
D512 HZS27-2
I502 BA4558
-12V
Q820 2SA1207
Q822 2SA1207
Q821 2SA1207
D822 1SS270A
D824 1SS270A
D821 1SS270A
Q824 DTC124ES
Q823 DTC124ES
D827 HZS7A1
MUTE

SYM.	REVISIONS	DATE	REVD.	CHKD.	APPD.
1					
2					
3					
4					
5					

Apply:
CM81*ETPlus-301
CM81*ETPlus-SNI

REGD.	DWN.	T. Hiaki	99·8·10	TITLE	Hitachi, Ltd.	YOKOHAMA WORKS DWG. No.	SH.
REGD. 99.8.13	CHKD.		·/·	DJ81A(HHEE)DEF CIRCUIT DIAGRAM	Tokyo Japan	327 W161703	01/01
	APPD.		·/				

REV.

100

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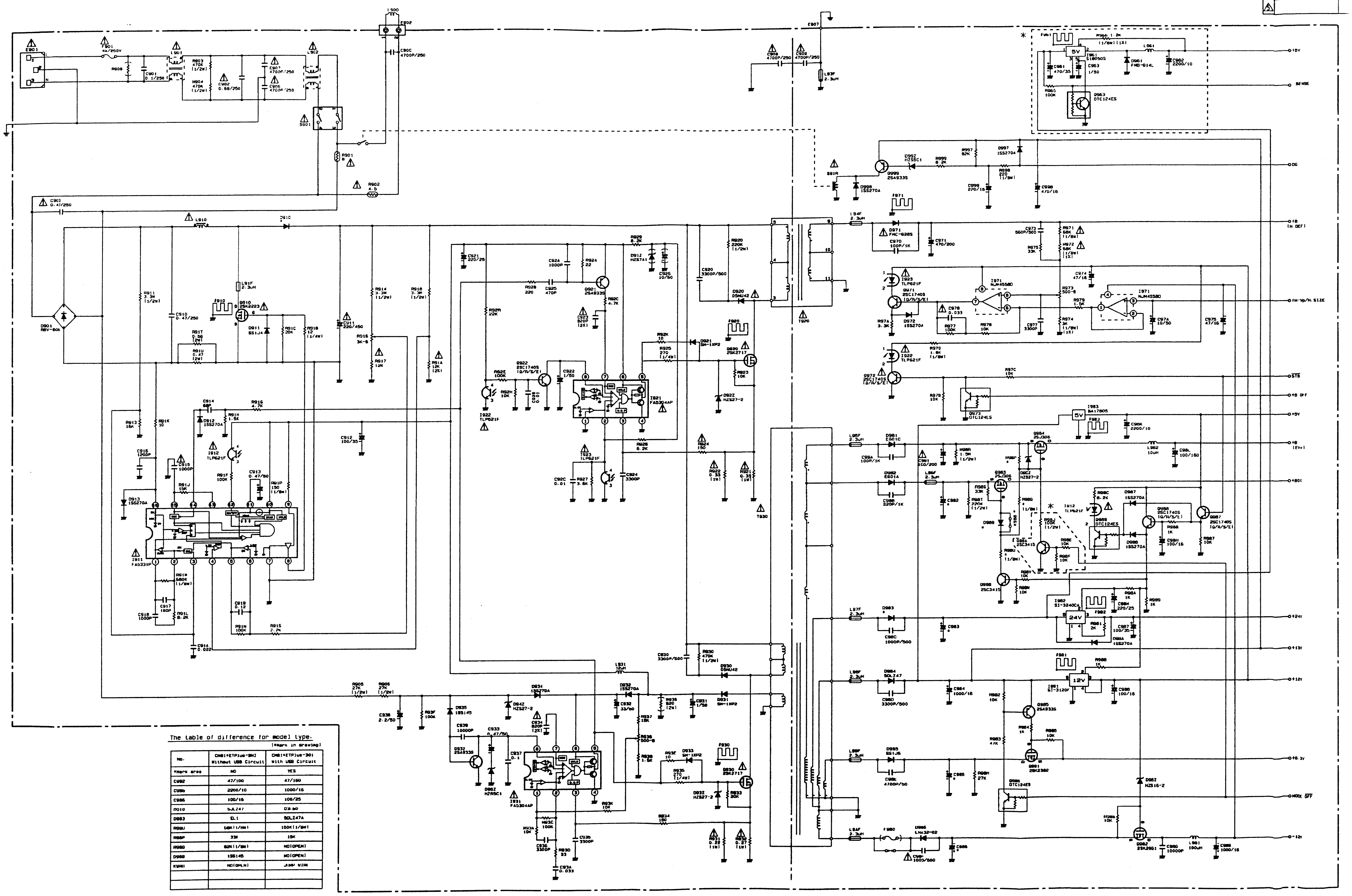
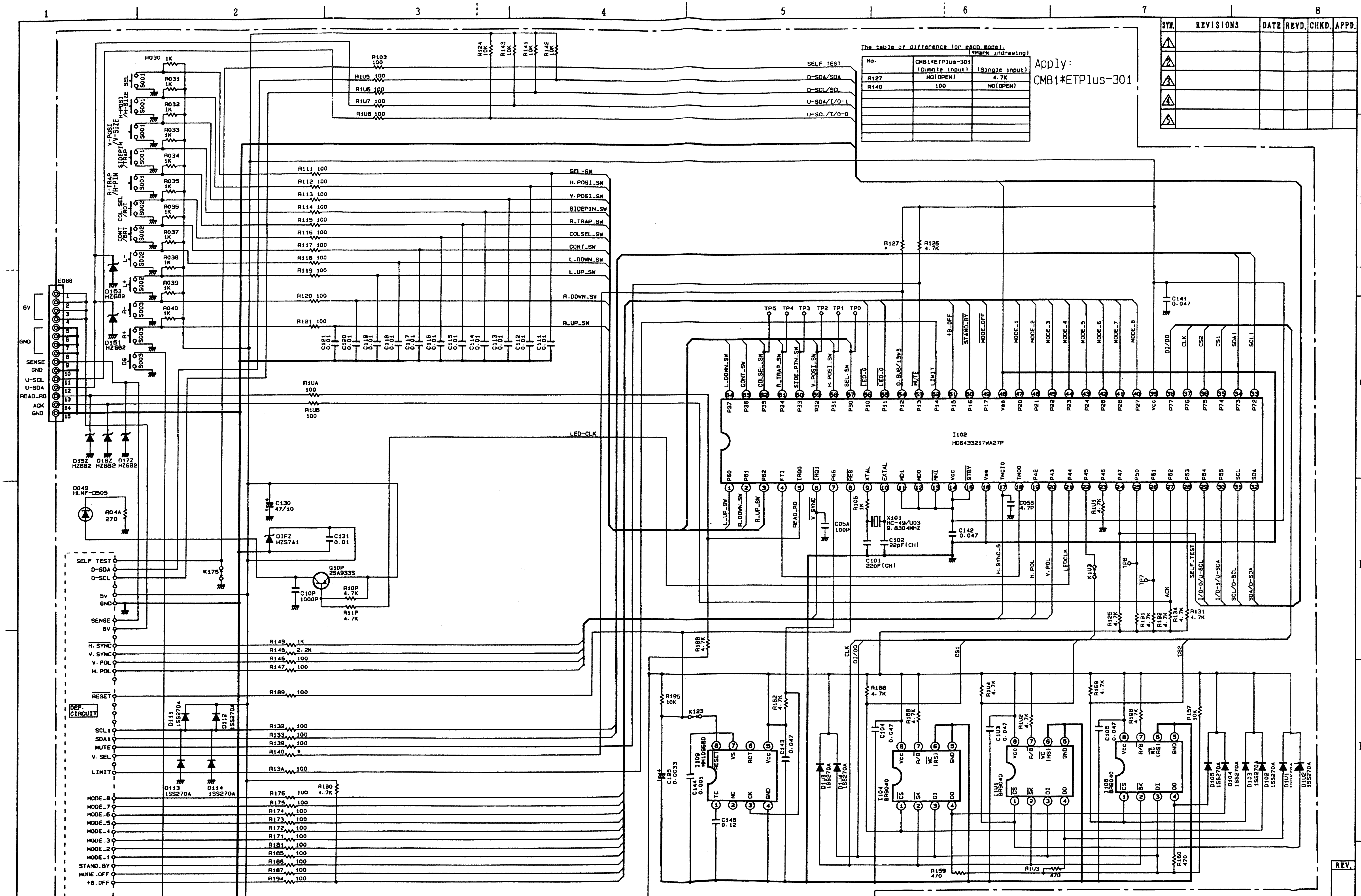

E901
F901 4A/250V
L901
L902
S901
R901
R902 4.5
C903 0.47/250
D901 RBV-606
L910
D910
Q910 2SK2223
L91F 2.3uH
I911 FA5331P
I912 TLP621F
I921 FA5304AP
I922 TLP621F
I923 TLP621F
Q920 2SK2717
Q921 2SA933S
Q922 2SC1740S
T920
T930
I931 FA5304AP
Q930 2SK2717
Q932 2SA933S
E907
L93F 2.3uH
I961 S1805DS
Q963 DTC124ES
Q999 2SA933S
I971 NJM4558D
I983 BA17805
I982 SI-3240CA
I981 SI-3120F
Q981 2SK2382
Q982 2SK2651
+15V
SENSE
DG
+B
(H DEF)
FH-Vp/H.SIZE
STB
+B OFF
+5V
+B
(Ehv)
+80V
+24V
+13V
+12V
+6.3V
MODE OFF
-12V

The table of difference for model type.

(*Mark in drawing)

No.	CM81*ETPlus-SNI Without USB Circuit	CM81*ETPlus-301 With USB Circuit
*Mark area	NO	YES
C982	47/100	47/160
C986	2200/10	1000/16
C986	100/16	100/25
D910	5JL247	D3.6D
D983	EL1	SOL247A
R98U	68K(1/8W)	100K(1/8W)
R98P	33K	15K
R980	82K(1/8W)	NO(OPEN)
D989	1SS146	NO(OPEN)
K9HH	NO(OPEN)	JUMP WIRE


E068
6V
GND
SENSE
GND
U-SCL
U-SDA
READ_RQ
ACK
GND
SEL
H-POSI /H-SIZE
V-POSI /V-SIZE
SIDEPIN /TRAP
R-TRAP /R-PIN
COL_SEL /ROT
CONT /BRI
L-
L+
R-
R+
DG
S001
S002
S003
R030 1K
R031 1K
R032 1K
R033 1K
R034 1K
R035 1K
R036 1K
R037 1K
R038 1K
R039 1K
R040 1K
D153 HZ6B2
D151 HZ6B2
D15Z HZ6B2
D16Z HZ6B2
D17Z HZ6B2
D049 HLMF-D505
R04A 270
R103 100
R1U5 100
R1U6 100
R1U7 100
R1U8 100
R124 10K
R143 10K
R141 10K
R142 10K
SELF TEST
D-SDA/SDA
D-SCL/SCL
U-SDA/I/O-1
U-SCL/I/O-0
R111 100
R112 100
R113 100
R114 100
R115 100
R116 100
R117 100
R118 100
R119 100
R120 100
R121 100
SEL-SW
H.POSI_SW
V.POSI_SW
SIDEPIN_SW
R_TRAP_SW
COLSEL_SW
CONT_SW
L_DOWN_SW
L_UP_SW
R_DOWN_SW
R_UP_SW
C121 0.01
C120 0.01
C119 0.01
C118 0.01
C117 0.01
C116 0.01
C115 0.01
C114 0.01
C113 0.01
C112 0.01
C111 0.01
R1UA 100
R1U8 100
LED-CLK
C130 47/10
D1FZ HZS7A1
C131 0.01
Q10P 2SA933S
C10P 1000P
R10P 4.7K
R11P 4.7K
K175
SELF TEST
D-SDA
D-SCL
5V
GND
SENSE
6V
H.SYNC
V.SYNC
V.POL
H.POL
RESET
DEF. CIRCUIT
SCL1
SDA1
MUTE
V.SEL
LIMIT
MODE_8
MODE_7
MODE_6
MODE_5
MODE_4
MODE_3
MODE_2
MODE_1
STAND_BY
MODE_OFF
+B_OFF
DG
R149 1K
R148 2.2K
R146 100
R147 100
R189 100
D111 1SS270A
D112 1SS270A
D113 1SS270A
D114 1SS270A
R132 100
R133 100
R139 100
R140 *
R13A 100
R176 100
R180 4.7K
R175 100
R174 100
R173 100
R172 100
R171 100
R181 100
R185 100
R186 100
R187 100
R194 100
TP5
TP4
TP3
TP2
TP1
TP0
R127 *
R126 4.7K
C141 0.047
L_DOWN_SW
CONT_SW
COLSEL_SW
R_TRAP_SW
SIDE_PIN_SW
V_POSI_SW
H_POSI_SW
SEL_SW
LED_G
LED_O
D.SUB/13W3
MUTE
LIMIT
+B_OFF
STAND_BY
MODE_OFF
MODE_1
MODE_2
MODE_3
MODE_4
MODE_5
MODE_6
MODE_7
MODE_8
DI/DO
CLK
CS2
CS1
SDA1
SCL1
P37
P36
P35
P34
P33
P32
P31
P30
P10
P11
P12
P13
P14
P15
P16
P17
Vss
P20
P21
P22
P23
P24
P25
P26
P27
Vcc
P77
P76
P75
P74
P73
P72
I102
HD6433217WA27P
P50
P51
P52
FTI
IRQ0
IRQ1
P66
RES
XTAL
EXTAL
MD1
MD0
NMI
Vcc
STBY
Vss
TMCI0
TMO0
P42
P43
P44
P45
P46
P47
P50
P51
P52
P53
P54
P55
SCL
SDA
L_UP_SW
R_DOWN_SW
R_UP_SW
READ_RQ
V_SYNC
C05A 100P
R106 1K
X101 HC-49/U03 9.8304MHZ
C102 22pF(CH)
C101 22pF(CH)
C142 0.047
C05B 4.7P
H.SYNC_B
H.POL
V.POL
LEDCLK
K1U3
R1U1 4.7K
TP6
TP7
ACK
SELF TEST
I/O-0/U-SCL
I/O-1/U-SDA
SCL/D-SCL
SDA/D-SDA
R125 4.7K
R191 4.7K
R192 4.7K
R134 4.7K
R131 4.7K
R188 4.7K
CLK
DI/DO
CS1
CS2
R195 10K
K123
R162 4.7K
C143 0.047
C185 0.0033
C144 0.001
I109 HM10956D
RESET
VS
RCT
Vcc
TC
NC
CK
GND
C145 0.12
D1U3 1SS270A
D1U4 1SS270A
R168 4.7K
C104 0.047
R158 4.7K
I104 BR9040
Vcc
R/B
WC (RS)
GND
CS
SK
DI
DO
R1U4 4.7K
C1U3 0.047
R1U2 4.7K
I1U1 BR9040
R169 4.7K
C105 0.047
R198 4.7K
I108 BR9040
R157 10K
D105 1SS270A
D104 1SS270A
D103 1SS270A
D102 1SS270A
D1U1 1SS270A
D1U2 1SS270A
R159 470
R1U3 470
R160 470
1
2
3
4
5
6
7
8
A
B
C
D
E
F

SYM.	REVISIONS	DATE	REVD.	CHKD.	APPD.
1					
2					
3					
4					
5					

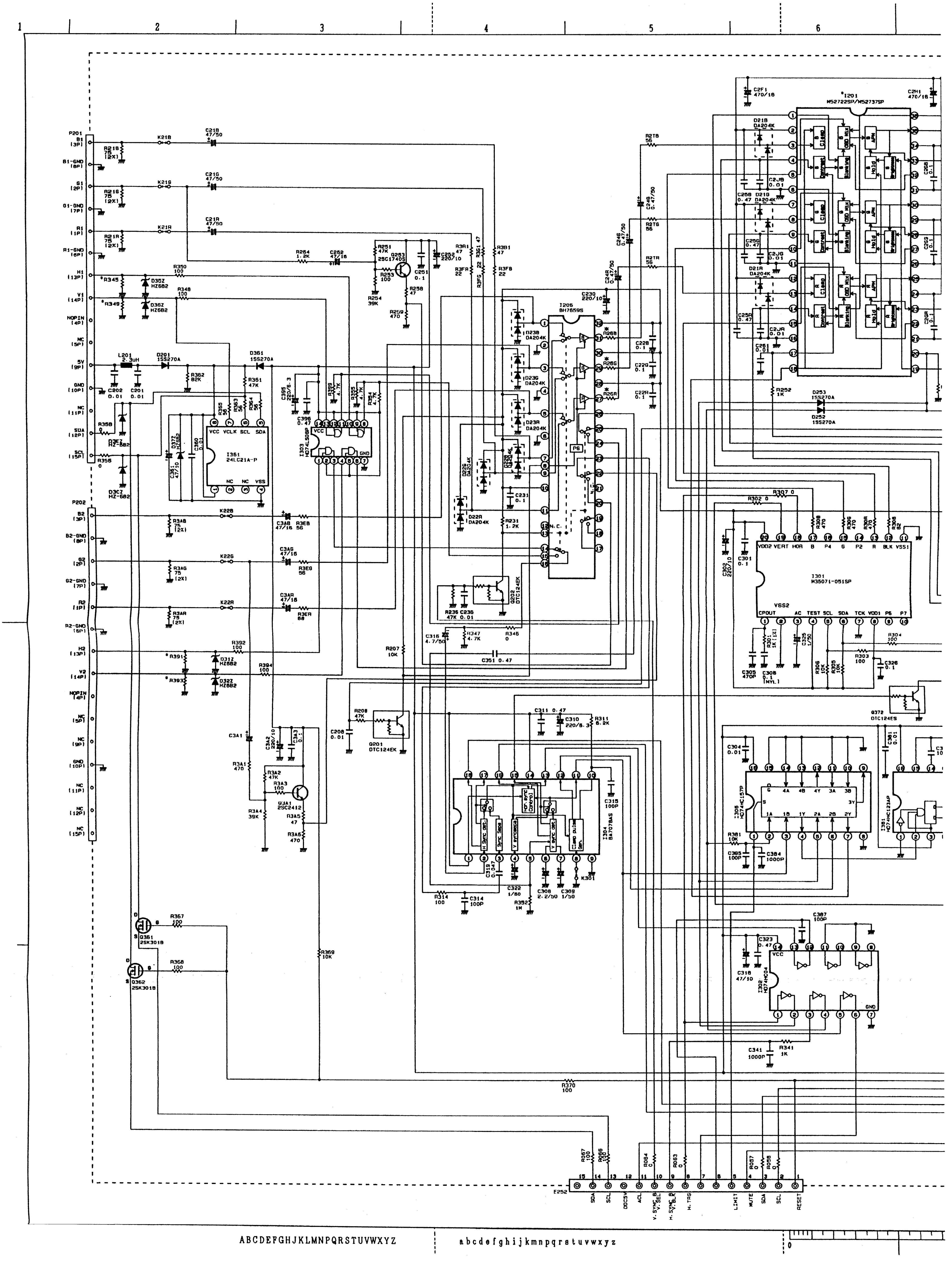
The table of difference for each model.
(*Mark indrawing)

No.	CM81*ETPlus-301 (Dubble input)	(Single input)
R127	NO(OPEN)	4.7K
R140	100	NO(OPEN)

Apply:
CM81*ETPlus-301

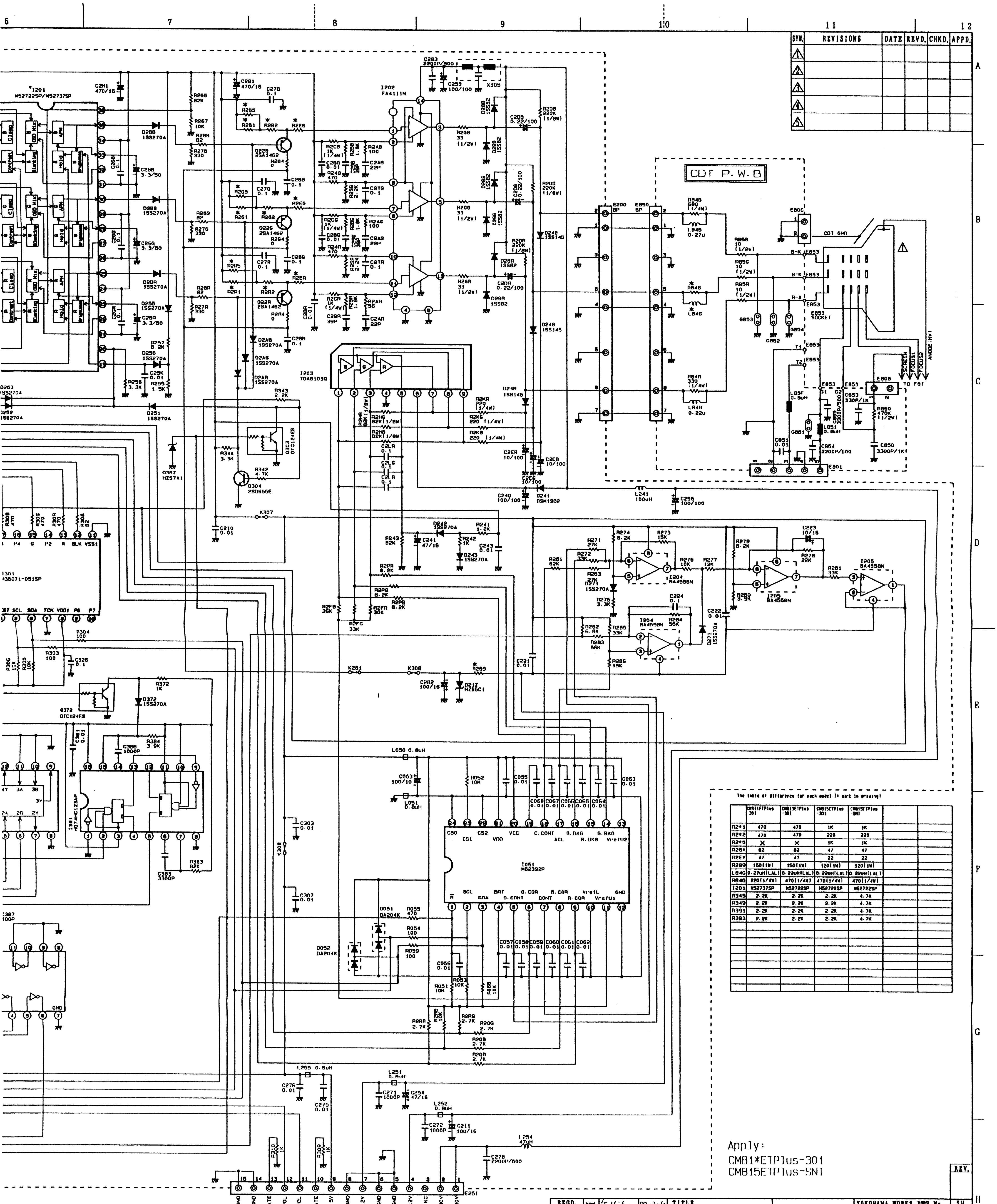
REGD.	DWN.	T. Higo	99.2.10	TITLE DJ81A(HHEE)MPU Circuit Diagram	Hitachi, Ltd. Tokyo Japan	YOKOHAMA WORKS DWG. No. 327 W161705	SH. 01/02
REGD. '99.3.19	CHKD.						
	APPD.						

REV.


1
2
3
4
5
6
P201
B1 (3P)
B1-GND (8P)
G1 (2P)
G1-GND (7P)
R1 (1P)
R1-GND (6P)
H1 (13P)
V1 (14P)
NOPIN (4P)
NC (5P)
5V (9P)
GND (10P)
NC (11P)
SDA (12P)
SCL (15P)
P202
B2 (3P)
B2-GND (8P)
G2 (2P)
G2-GND (7P)
R2 (1P)
R2-GND (6P)
H2 (13P)
V2 (14P)
NOPIN (4P)
NC (5P)
NC (9P)
GND (10P)
NC (11P)
NC (12P)
NC (15P)
K21B
K21G
K21R
C21B 47/50
C21G 47/50
C21R 47/50
R21B 75 (2X)
R21G 75 (2X)
R21R 75 (2X)
R350 100
R348 100
R345
R349
D35Z HZ6B2
D36Z HZ6B2
L201 2.2uH
D201 1SS270A
D361 1SS270A
R362 82K
R361 47K
C202 0.01
C201 0.01
R358
D3EZ HZ-6B2
D3CZ HZ-6B2
R356 0
R355 56
R363 56
R364 56
D372 HZ6B2
C361 47/10
C360 0.01
I361 24LC21A-P
VCC VCLK SCL SDA
NC NC VSS
R264 1.2K
C262 47/16
R251 47K
Q253 2SC1740S
R253 100
R254 39K
R258 47
R259 470
C251 0.1
C252 220/10
R3A1 47
R3G1 47
R3B1 47
R3FA 22
R3FG 22
R3FB 22
C395 220/6.3
C396 0.47
R399 4.7K
R355 4.7K
R354 4.7K
I303 HD74LS08P
VCC GND
D23B DA204K
D23G DA204K
D23R DA204K
D22G DA204K
D22B DA204K
D22R DA204K
I205 BH7659S
C230 220/10
C24R 0.47/50
C24G 0.47/50
C24B 0.47/50
R26B
R26G
R26R
C22B 0.1
C22G 0.1
C22R 0.1
R2TB 56
R2TG 56
R2TR 56
P6
N.C.
C231 0.1
R231 1.2K
R236 47K
C236 0.01
Q202 DTC124EK
C316 4.7/50
R347 4.7K
R346 0
R207 10K
C351 0.47
K22B
K22G
K22R
R3AB 75 (2X)
R3AG 75 (2X)
R3AR 75 (2X)
C3AB 47/16
C3AG 47/16
C3AR 47/16
R3EB 56
R3EG 56
R3ER 68
R392 100
R394 100
R391
R393
D31Z HZ6B2
D32Z HZ6B2
C3A1
C3A2 220/10
C3A3 0.1
R3A1 470
R3A2 47K
R3A3 100
Q3A1 2SC2412
R3A4 39K
R3A5 47
R3A6 470
R208 47K
C208 0.01
Q201 DTC124EK
C311 0.47
C310 220/6.3
R311 8.2K
I304 BA7078AS
H sync det.
Sync Sepa
V sync sepa
Hor. sync control
V sync det.
Clamp pulse gen.
C315 100P
C319 0.047
C322 1/50
C308 2.2/50
C309 1/50
K301
R314 100
C314 100P
R352 1M
R357 100
Q361 2SK3018
R368 100
Q362 2SK3018
R369 10K
R370 100
C2F1 470/16
C2H1 470/16
I201 M52722SP/M52737SP
D21B DA204K
D21G DA204K
D21R DA204K
C25B 0.47
C25G 0.47
C25R 0.47
C2JB 0.01
C2JG 0.01
C2JR 0.01
C261 0.01
B Clamp
B Contrast
B OSD Mix
B Blanking
B APH
B Hold
B Brightness
G Clamp
G Contrast
G OSD Mix
G Blanking
G APH
G Hold
G Brightness
R Clamp
R Contrast
R OSD Mix
R Blanking
R APH
R Hold
R Brightness
C26B 0.1
C2G3 0.1
C2GR 0.1
R252 1K
D253 1SS270A
D252 1SS270A
R302 0
R307 0
R308 470
R306 470
R30R 470
R305 82
C302 220/10
C301 0.1
VDD2 VERT HOR B P4 G P2 R BLK VSS1
I301 M35071-051SP
VSS2
CPOUT AC TEST SCL SDA TCK VDD1 P6 P7
R301 1K (1X)
C325 1/50
C305 470P
C308 0.1 (MYL)
R306 10K
R305 10K
R303 100
R304 100
C326 0.1
Q372 DTC124ES
C304 0.01
I305 HD74HC157P
G 4A 4B 4Y 3A 3B
S 3Y
1A 1B 1Y 2A 2B 2Y
R381 10K
C385 100P
C384 1000P
C381 0.1
I381 HD74HC123AP
C387 100P
C323 0.47
C318 47/10
I302 HD74HC04
VCC
GND
C341 1000P
R341 1K
R067 100
R066 100
R064 0
R063 0
R057 0
R056 0
R055 0
E252
SDA
SCL
DDC5V
ACL
V.SYNC_B V.SEL
H.SYNC_B V.BLK
H.TRG
LIMIT
MUTE
SDA
SCL
RESET

ABCDEFGHJKLMNPQRSTUVWXYZ

abcdefghijkmnpqrstuvwxyz


6
7
8
9
10
11
12
A
B
C
D
E
F
G
H
I201 M52722SP/M52737SP
I202 FA4111M
I203 TDA6103Q
I301 435071-051SP
I381 M74HC123AP
I051 M52392P
I204 BA4558N
I205 BA4558N
Q22B 2SA1462
Q22G 2SA1462
Q22R 2SA1462
Q303 DTC124ES
Q304 2SD655E
Q372 DTC124ES
CDT P.W.B
E200 8P
E850 8P
E800
E853 SOCKET
E801
E808
CDT GND
SCREEN
FOCUS1
FOCUS2
ANODE(HV)
TO FBT
B-K
G-K
R-K
K307
K308
K281
L241 100uH
L050 0.8uH
L255 0.8uH
L251 0.8uH
L252 0.8uH
L254 47uH
E251
GND
GND
V.STATE
H.POL
V.POL
H.STATE
5V
GND
-12V
GND
GND
12V
NC
80V
90V

STM.	REVISIONS	DATE	REVD.	CHKD.	APPD.
⚠1					
⚠2					
⚠3					
⚠4					
⚠5					

The table of difference (or each model.)(* mark in drawing)

	CM811ETPlus 301	CM813ETPlus -301	CM815ETPlus -301	CM815ETPlus -SNI		
R2*1	470	470	1K	1K		
R2*2	470	470	220	220		
R2*5	X	X	1K	1K		
R26*	82	82	47	47		
R2E*	47	47	22	22		
R289	150(1W)	150(1W)	120(1W)	120(1W)		
L84G	0.27uH(LAL)	0.22uH(LAL)	0.22uH(LAL)	0.22uH(LAL)		
R84G	820(1/4W)	470(1/4W)	470(1/4W)	470(1/4W)		
I201	M52737SP	M52722SP	M52722SP	M52722SP		
R345	2.2K	2.2K	2.2K	4.7K		
R349	2.2K	2.2K	2.2K	4.7K		
R391	2.2K	2.2K	2.2K	4.7K		
R393	2.2K	2.2K	2.2K	4.7K		

Apply:
CM81*ETPlus-301
CM815ETPlus-SNI

REGD.	DWN.	T. Hioki	93.2.10	TITLE DJ81A(HHEE)VIDEO CIRCUIT DIAGRAM	**Hitachi, Ltd.** Tokyo Japan	YOKOHAMA WORKS DWG. No. 327W161704	REV. SH. 01/02
	CHKD.						
	APPD.						

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